



dscal
DIGITAL SYSTEMS & COMPUTER ARCHITECTURE LABORATORY

Εργαστήριο Λογικής Σχεδίασης

4^ο Εργαστηριακό Μάθημα

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4^η Εργαστηριακή Άσκηση

Ανάλυση άσκησης

Δημιουργία νέου Ρολογιού
=
100 εκ. χτύποι του CLK της
κάρτας

Υπολογισμός επόμενης κατάστασης

Ενημέρωση Τρέχουσας Κατάστασης

Υπολογισμός εξόδου

4^η Εργαστηριακή Άσκηση

ΠΡΟΧΩΡΗΣΤΕ ΣΤΗΝ ΑΣΚΗΣΗ



4^η Εργαστηριακή Άσκηση

Αρχιτεκτονική (1/3) – Νέο Ρολόι (Περίοδος = 1 sec)

Αρχιτεκτονική



```
One_sec_clk : process (clk, reset) is
variable clk_ticks : integer;

begin
    if reset = '1' then
        clk_100MHz<='0';
        clk_ticks :=0;
    elsif rising_edge(clk) then
        if clk_ticks = 99999999 then
            clk_ticks := 0;
            clk_100MHz<= '1';
        else
            clk_ticks := clk_ticks + 1;
            clk_100MHz <= '0';
        end if; -- clk_ticks
    end if; --reset
end process One_sec_clk;
```

4^η Εργαστηριακή Άσκηση

Αρχιτεκτονική (2/3) – Tick Counter

Αρχιτεκτονική 

```
count: process (clk_100MHz, reset) is
begin
  if (reset='1') then
    counts<=(others=>'0');
  elsif rising_edge(clk_100MHz) then
    if direction='1' then
      if counts<9 then
        counts<=counts+1;
      else
        counts<=(others=>'0'); -- -- count<="0000";
      end if; -- counts<9
    else
      if counts>0 then
        counts<=counts-1;
      else
        counts<="1001";
      end if; -- counts>0
    end if; --direction
  end if; --reset
end process count;
```

4^η Εργαστηριακή Άσκηση

Αρχιτεκτονική (3/3) – Output signals

Αρχιτεκτονική 

```
led_result<=std_logic_vector(counts);
```

```
counts_digit_values: process (counts) begin
```

```
case counts is
```

```
  when X"0" => seven_segment <="0111111"; -- 0
```

```
  when X"1" => seven_segment <="0000110"; -- 1
```

```
  when X"2" => seven_segment <="1011011"; -- 2
```

```
  when X"3" => seven_segment <="1001111"; -- 3
```

```
  when X"4" => seven_segment <="1100110"; -- 4
```

```
  when X"5" => seven_segment <="1101101"; -- 5
```

```
  when X"6" => seven_segment <="1111101"; -- 6
```

```
  when X"7" => seven_segment <="0000111"; -- 7
```

```
  when X"8" => seven_segment <="1111111"; -- 8
```

```
  when X"9" => seven_segment <="1101111"; -- 9
```

```
  when others => seven_segment <="0000000";
```

```
end case;
```

```
end process counts_digit_values;
```

```
digit_selection_out<=digit_selection_in;
```

4^η Εργαστηριακή Άσκηση

Constraints (1/2) – CLK + Switches + Leds

```
# CLK - Zedboard 100MHz oscillator  
set_property -dict { PACKAGE_PIN Y9 IOSTANDARD LVCMOS33 } [get_ports {clk}]
```

```
#####  
# On-board Slide Switches #  
#####
```

Constraints →

```
set_property -dict { PACKAGE_PIN M15 IOSTANDARD LVCMOS33 } [get_ports { digit_selection_in }];  
set_property -dict { PACKAGE_PIN H17 IOSTANDARD LVCMOS33 } [get_ports { reset }];  
set_property -dict { PACKAGE_PIN F22 IOSTANDARD LVCMOS33 } [get_ports { direction }];
```

```
#####  
# On-board LEDS #  
#####
```

```
set_property -dict { PACKAGE_PIN T22 IOSTANDARD LVCMOS33 } [get_ports { led_result[0] }];  
set_property -dict { PACKAGE_PIN T21 IOSTANDARD LVCMOS33 } [get_ports { led_result[1] }];  
set_property -dict { PACKAGE_PIN U22 IOSTANDARD LVCMOS33 } [get_ports { led_result[2] }];  
set_property -dict { PACKAGE_PIN U21 IOSTANDARD LVCMOS33 } [get_ports { led_result[3] }];
```

4^η Εργαστηριακή Άσκηση

Constraints (1/2) – Pmod

```
#####  
# PmodSSO          #  
#####
```

```
set_property -dict { PACKAGE_PIN Y11  IOSTANDARD LVCMOS33 } [get_ports { seven_segment[0] }];  
set_property -dict { PACKAGE_PIN AA11 IOSTANDARD LVCMOS33 } [get_ports { seven_segment[1] }];  
set_property -dict { PACKAGE_PIN Y10  IOSTANDARD LVCMOS33 } [get_ports { seven_segment[2] }];  
set_property -dict { PACKAGE_PIN AA9  IOSTANDARD LVCMOS33 } [get_ports { seven_segment[3] }];  
set_property -dict { PACKAGE_PIN W12  IOSTANDARD LVCMOS33 } [get_ports { seven_segment[4] }];  
set_property -dict { PACKAGE_PIN W11  IOSTANDARD LVCMOS33 } [get_ports { seven_segment[5] }];  
set_property -dict { PACKAGE_PIN V10  IOSTANDARD LVCMOS33 } [get_ports { seven_segment[6] }];
```

```
set_property -dict { PACKAGE_PIN W8  IOSTANDARD LVCMOS33 } [get_ports { digit_selection_out }];
```

```
#####
```

```
##ZedBoard Timing Constraints
```

```
#####
```

```
# define clock and period
```

```
create_clock -period 10 -name CLK -waveform {0.000 5.000} [get_ports {clk}]
```

Constraints



4^η Εργαστηριακή Άσκηση

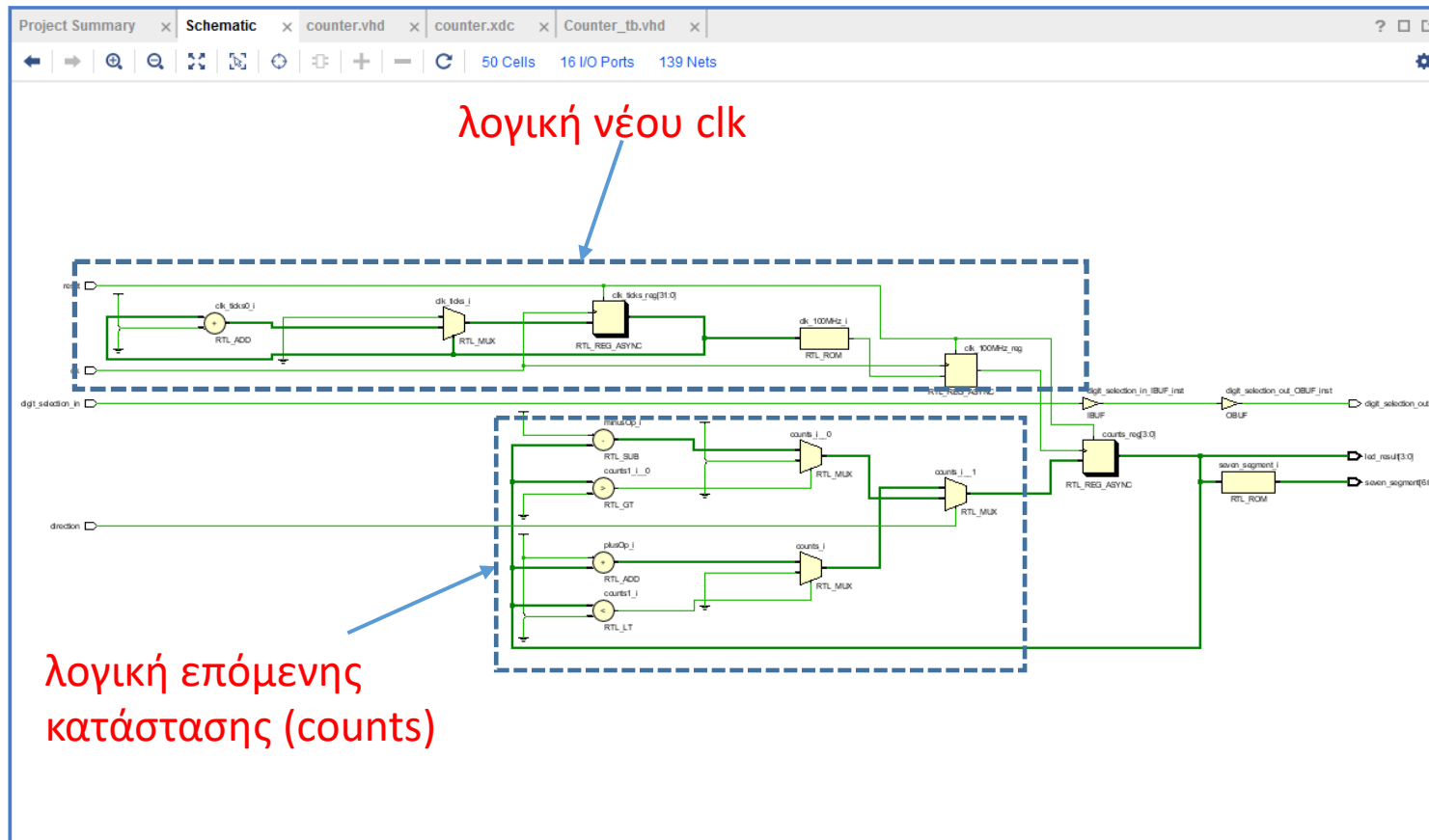
Pmod Manual

Manual Pmod

<https://reference.digilentinc.com/reference/pmod/pmodssd/reference-manual>

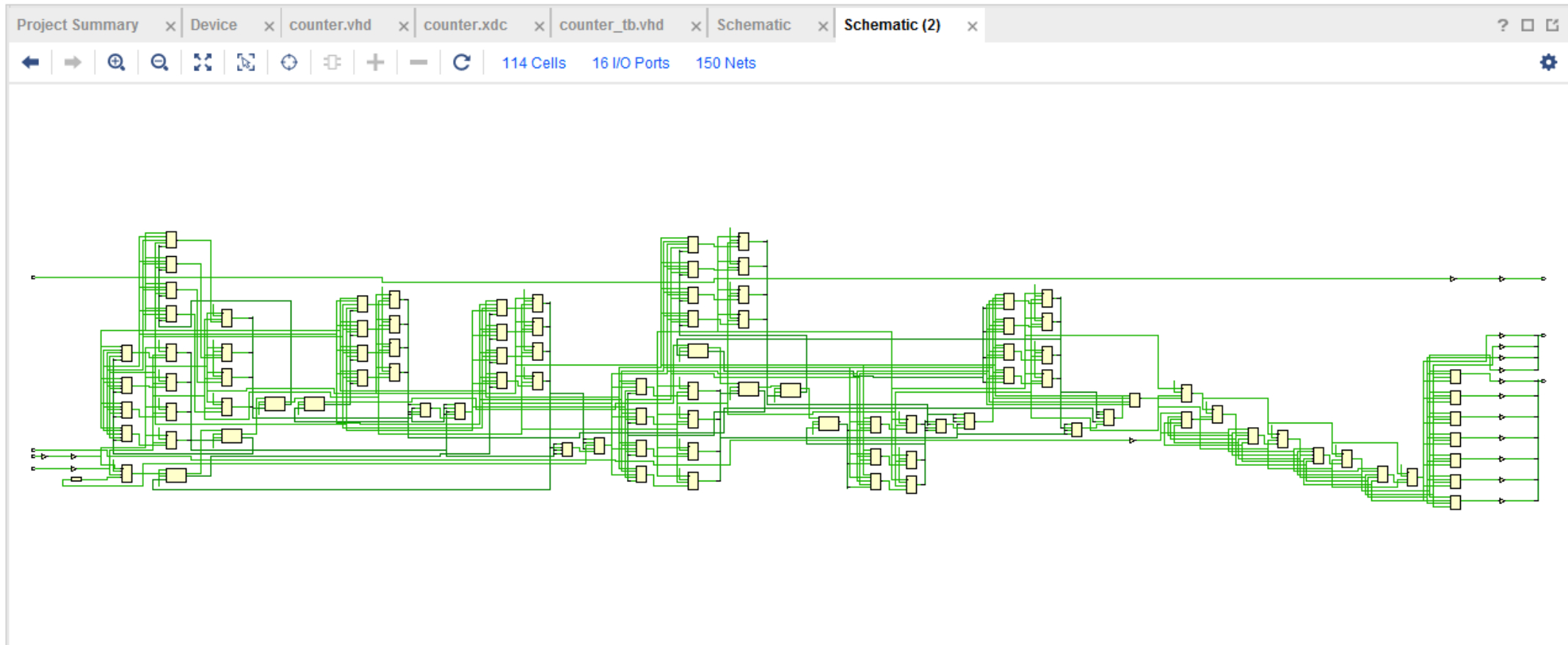
4^η Εργαστηριακή Άσκηση

RTL Design



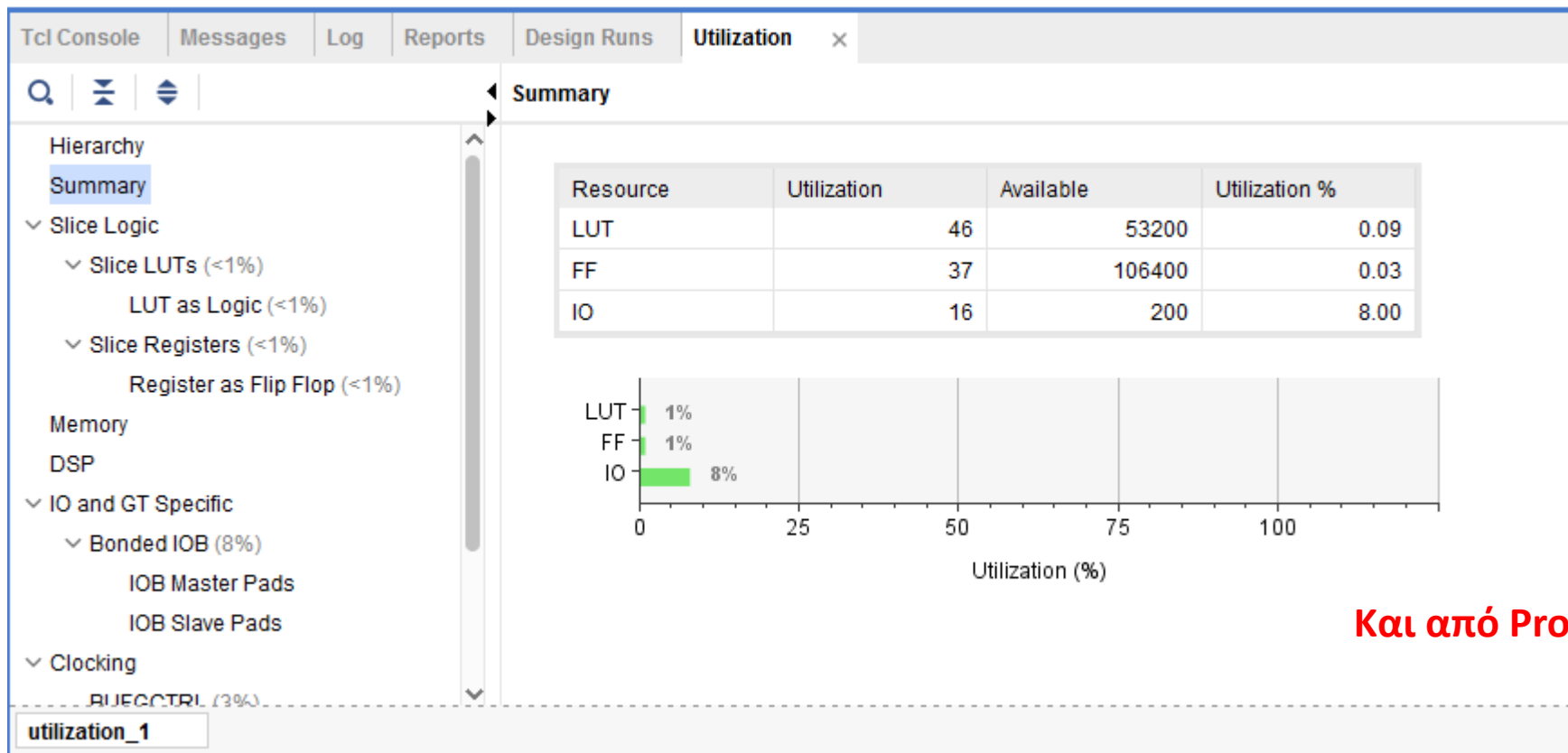
4^η Εργαστηριακή Άσκηση

Synthesis/Implementation – Schematic



4^η Εργαστηριακή Άσκηση

Implementation – Report Utilization



Και από Project Summary

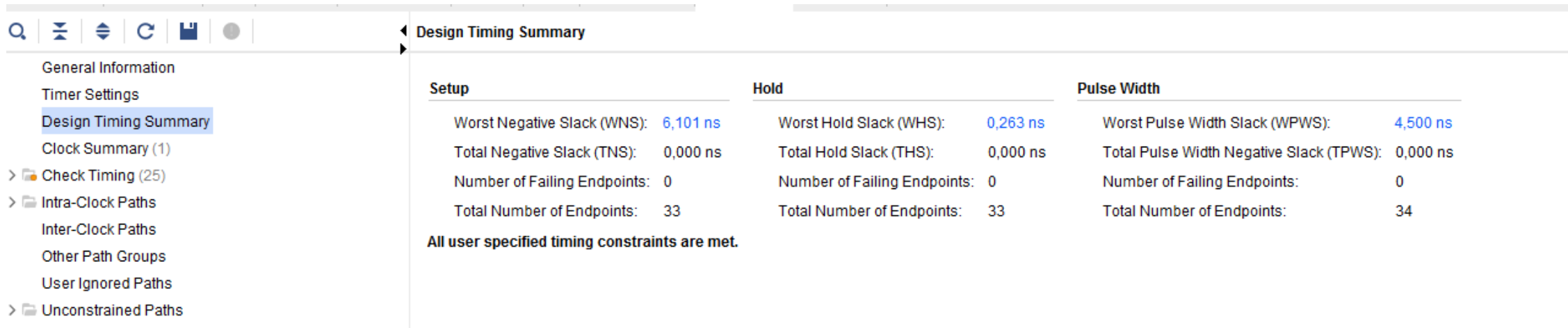
4^η Εργαστηριακή Άσκηση

Implementation – Timing Reports (1/4)

Menu Reports->Timing-> Report Timing Summary

ή

Open Implemented Design->Report Timing Summary



The screenshot shows the 'Design Timing Summary' report. The left sidebar contains a navigation tree with the following items: General Information, Timer Settings, Design Timing Summary (highlighted), Clock Summary (1), Check Timing (25), Intra-Clock Paths, Inter-Clock Paths, Other Path Groups, User Ignored Paths, and Unconstrained Paths. The main content area displays a table with three columns: Setup, Hold, and Pulse Width. The table contains the following data:

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 6,101 ns	Worst Hold Slack (WHS): 0,263 ns	Worst Pulse Width Slack (WPWS): 4,500 ns
Total Negative Slack (TNS): 0,000 ns	Total Hold Slack (THS): 0,000 ns	Total Pulse Width Negative Slack (TPWS): 0,000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 33	Total Number of Endpoints: 33	Total Number of Endpoints: 34

Below the table, the text states: **All user specified timing constraints are met.**

4^η Εργαστηριακή Άσκηση

Implementation – Timing Reports (2/4)

The screenshot displays a digital design tool interface. The top window shows a schematic diagram with various logic components and interconnecting nets. The bottom window shows a timing report for 'Intra-Clock Paths - CLK - Setup'.

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock	Excep
Path 1	6.027	3	3	32	One_sec_clk.clk_ticks_reg[29]/C	One_sec_clk.clk_ticks_reg[3]/D	3.939	0.828	3.111	10.0	CLK	CLK	
Path 2	6.033	3	3	32	One_sec_clk.clk_ticks_reg[29]/C	One_sec_clk.clk_ticks_reg[6]/D	3.932	0.828	3.104	10.0	CLK	CLK	
Path 3	6.117	3	3	32	One_sec_clk.clk_ticks_reg[29]/C	One_sec_clk.clk_ticks_reg[12]/D	3.848	0.828	3.020	10.0	CLK	CLK	
Path 4	6.163	9	2	2	One_sec_clk.clk_ticks_reg[2]/C	One_sec_clk.clk_ticks_reg[31]/D	3.816	2.355	1.461	10.0	CLK	CLK	
Path 5	6.183	3	3	32	One_sec_clk.clk_ticks_reg[5]/C	One_sec_clk.clk_ticks_reg[27]/D	3.795	0.828	2.967	10.0	CLK	CLK	
Path 6	6.186	3	3	32	One_sec_clk.clk_ticks_reg[29]/C	One_sec_clk.clk_ticks_reg[8]/D	3.781	0.828	2.953	10.0	CLK	CLK	
Path 7	6.260	3	3	32	One_sec_clk.clk_ticks_reg[29]/C	One_sec_clk.clk_ticks_reg[7]/D	3.707	0.828	2.879	10.0	CLK	CLK	
Path 8	6.321	8	2	2	One_sec_clk.clk_ticks_reg[2]/C	One_sec_clk.clk_ticks_reg[25]/D	3.656	2.212	1.444	10.0	CLK	CLK	
Path 9	6.330	7	2	2	One_sec_clk.clk_ticks_reg[2]/C	One_sec_clk.clk_ticks_reg[24]/D	3.648	2.203	1.445	10.0	CLK	CLK	
Path 10	6.358	8	2	2	One_sec_clk.clk_ticks_reg[2]/C	One_sec_clk.clk_ticks_reg[28]/D	3.621	2.320	1.301	10.0	CLK	CLK	

Setup Time:

Αναφέρεται στις αργές διαδρομές (καθυστέρηση διάδοσης)

4^η Εργαστηριακή Άσκηση

Implementation – Timing Reports (3/4)

The screenshot displays the Xilinx Vivado interface for a project named 'IMPLEMENTED DESIGN - xc7z020dgg484-1'. The main window shows a schematic diagram of a counter circuit with various components like LUTs, registers, and multiplexers. A path is highlighted in blue, corresponding to the entry in the timing report below.

Path Properties

Property	Value
Name	Path 1
Slack (Hold)	0.263ns
Source	clk_ticks_reg[0]C (rising edge-triggered)
Destination	clk_ticks_reg[0]D (rising edge-triggered)
Path Group	CLK
Path Type	Hold (Min at Fast Process Corner)

Timing Checks - Hold

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Logic %	Net %	Requirement	Source Clock	Destination Clock	Exception
Constrained Paths (1)															
CLK (10)															
Path 1	0.263	1	1	3	clk_ticks_reg[0]C	clk_ticks_reg[0]D	0.354	0.186	0.168	52.5	47.5	0.000	CLK	CLK	
Path 2	0.381	2	2	32	clk_ticks_reg[25]C	clk_ticks_reg[27]D	0.473	0.231	0.242	48.8	51.2	0.000	CLK	CLK	
Path 3	0.400	2	2	32	clk_ticks_reg[25]C	clk_ticks_reg[28]D	0.505	0.231	0.274	45.7	54.3	0.000	CLK	CLK	
Path 4	0.400	2	2	32	clk_ticks_reg[11]C	clk_ticks_reg[13]D	0.506	0.231	0.275	45.6	54.4	0.000	CLK	CLK	
Path 5	0.403	2	2	32	clk_ticks_reg[1]C	clk_ticks_reg[3]D	0.495	0.231	0.264	46.7	53.3	0.000	CLK	CLK	
Path 6	0.441	2	2	32	clk_ticks_reg[11]C	clk_ticks_reg[10]D	0.533	0.231	0.302	43.3	56.7	0.000	CLK	CLK	
Path 7	0.442	2	2	32	clk_ticks_reg[1]C	clk_ticks_reg[6]D	0.548	0.231	0.317	42.2	57.8	0.000	CLK	CLK	
Path 8	0.447	2	2	32	clk_ticks_reg[18]C	clk_ticks_reg[20]D	0.539	0.231	0.308	42.9	57.1	0.000	CLK	CLK	

Hold Time:

Αναφέρεται στις γρήγορες διαδρομές (καθυστέρηση μόλυνσης)

4^η Εργαστηριακή Άσκηση

Implementation – Timing Reports (4/4)

TCL Console>report_timing_summary –datasheet

The screenshot displays a digital design tool interface. On the left, there is a 'Sources' window showing a hierarchy of components including 'digit_selection_in', 'digit_selection_out', and various clock signals. Below it, the 'Net Properties' window shows details for the 'digit_selection_in' net. The main area is a 'Schematic (2)' window showing a complex circuit diagram with green traces and logic blocks. At the bottom, the 'Tcl Console' window displays the output of the 'report_timing_summary' command, showing a table of combinational delays.

From Port	To Port	Max Delay (ns)	Process Corner	Min Delay (ns)	Process Corner
digit_selection_in	digit_selection_out	10.817	SLOW	3.770	FAST

Προσοχή