



National and Kapodistrian University of Athens

dscal
DIGITAL SYSTEMS & COMPUTER ARCHITECTURE LABORATORY

State-of-the-art Space Upstream Technologies for Aerospace Applications

Payload Data Processing Units and High-Speed Hardware Accelerators
(FPGA/ASIC/IP cores) *Designed in Greece*

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DSCAL Resume

- The Digital Systems and Computer Architecture Laboratory (DSCAL) of the National and Kapodistrian University of Athens (NKUA) research team consists of faculty members and researchers from the School of Science, specifically from the Department of Informatics and Telecommunications (Professor A. Paschalis) and the Department of Aerospace Science and Technology (AST) (Professor N. Kranitis).
- The NKUA-DSCAL team serves the educational, research, and developmental needs of the NKUA's School of Science, focusing on the design and architecture of computing systems, as well as the interactions between hardware and software in terms of performance, energy/power consumption, and reliability for high-performance embedded systems. It covers hardware accelerator systems implemented in Field Programmable Gate Arrays (FPGAs) and Application Specific Integrated Circuits (ASICs).
- The research team's activities are focused on the development of On-board Data Systems, with an emphasis on Payload Data Processing, having participated in major institutional space missions of the European Space Agency (ESA) since 2009 (PROBA-3, TRUTHS), gaining valuable experience in microelectronics system design standards for space applications (ECSS-Q-ST-60-02C, ECSS-E-ST-20-40C) and achieving a high Technology Readiness Level and flight heritage (TRL-9 from PROBA-3 mission).
- Additionally, the team is involved in the ERMIS - Hellenic CubeSat Demonstration Mission with prime contractor the Department of Aerospace Science and technology of the National and Kapodistrian University of Athens that aims to develop in Greece 3 nanosatellites (6U-8U CubeSat type) under the Greek National Satellite Space Programme in order to demonstrate pilot activities like 5G-IoT communication services, RF inter-satellite link, optical laser link, hyperspectral EO applications, ADCS, OBC, Payload Data Processing Units and hardware accelerators of CCSDS algorithms, ground segment capabilities and skills, all unique to Greece and Europe, having undertaken the responsibility of developing in Greece the Payload Data Processing Unit for the ERMIS mission. The team also participates in five missions in total of the ESA/Greek National Space Programme and especially in Axis 1.2 (radar program) developing novel SAR raw data compression solutions.
- Committed to the vision of “Create a Center of Excellence in Space Upstream Technology Designed in Greece,” the NKUA-DSCAL research team can provide cutting-edge technologies and products to the global industry. These include Payload Data Processing Units and hardware accelerator IP cores for FPGA/ASIC technologies, implementing standards of the Consultative Committee for Space Data Systems (CCSDS).

DSCAL Core Business / Expertise

➤ ESA Technology Tree: On-Board Data Subsystems Domain

- Payload Data Processing (System, HW, SW, FW, Technologies) since 2010
 - System-On-Chip (SoC) Dependable and Adaptable Payload Data Processing Units (PDPU)
 - Hardware accelerators' firmware development in ASIC/FPGA/IP Core technology according to:
 - ECSS-Q-ST-60-02C "ASIC and FPGA development (31 July 2008)"
 - ECSS-E-ST-20-40C "ASIC, FPGA and IP Core engineering (11 October 2023)"
 - High-Speed Data Chain for "smart" next-generation payloads for Earth Observation, optical/RF com
 - Fault Detection, Isolation and Recovery (FDIR)
- Space Technology Heritage and High TRL from Space Missions (TRL=9, 2024)

Technical means:

- ✓ FPGA development boards (e.g. Zynq, Virtex-7, Ultrascale+) and GOMSpace Nanomind MK3 HP/SDR
- ✓ Workstations with state-of-the-art EDA CAD tools from AMD/Xilinx, Synopsys, Mentor Graphics and Microchip Technology
- ✓ 2GHz Mixed Signal Oscilloscope with 8-analog & 64-digital channels, power supplies, etc.
- ✓ End-to-end validation with SpaceFibre (ECSS-E-ST-50-11C) & SpaceWire (ECSS-E-ST-50-12C) Tester

Mature Space Upstream Technology in Space Missions

➤ ESA PROBA-3 Coronagraph System (2009-2024)

- Phases A/B/C/D/E1, Launch 12/2024, IOCR 7/25 – Mission completed successfully
- Image Data Compression Algorithm and HW accelerator (IP core in FPGA technology)
- Based on CCSDS 121 Lossless Data Compression
- **Flight heritage, TRL=9@2024** (DSCAL/CBK/CSL)

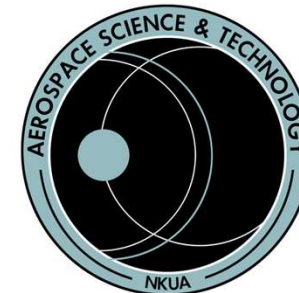


➤ ESA TRUTHS (2021-2025)

- Phases A/B1/B2
- System Feasibility Studies for On-Board Compression
- Implementation of CCSDS 123.0-B-2 Low-Complexity Lossless and Near-Lossless Multispectral and Hyperspectral Image Compression algorithm (participation in PPU implementation with ISD)
- **Now@TRL=4** (DSCAL/ISD/AIRBUS)

➤ ERMIS Hellenic CubeSat Demonstration Mission (2023-2026)

- Phase A/B/C/D/E1/E2
- IOD/IOV of Payload Data Processing Unit designed in Greece
- IOD/IOV of State-of-the-art HW accelerators of CCSDS algorithms:
 - CCSDS 123.0-B-2 lossless and near-lossless hyperspectral image compression,
 - CCSDS 122.0-B-2 image data compression
 - CCSDS 142.0-B-2 O3K LDPC channel-coding
- **Now@TRL=6, Expecting TRL9@Q1/2026** (DSCAL/DAST)

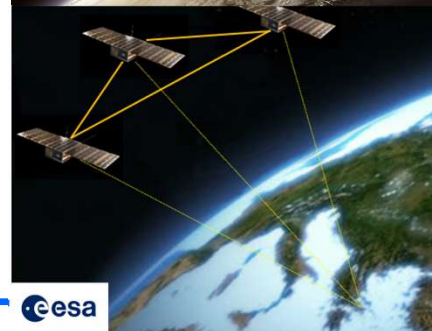


Participation in 4 more missions of National Space Program (2024-2026)

esa



esa



esa

The ESA Proba-3 mission

➤ Mission scope:

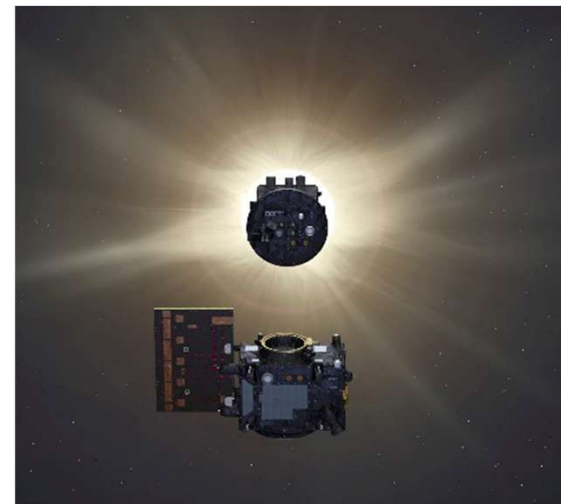
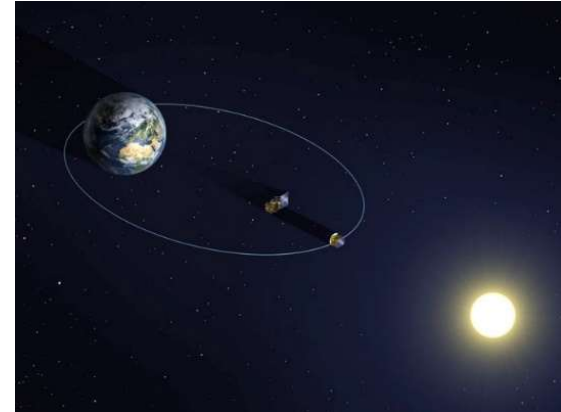
- To develop and demonstrate in-orbit the formation flying (FF) of two space-crafts (S/C)
- To develop and validate the engineering approach, ground verification tools and facilities required to achieve formation flying
- To provide scientific data using the **giant coronagraph system (ASPIICS)** for the observation of the sun corona

➤ Mission overview:

- Proba-3 mission consists of two S/C, the Coronagraph S/C and the Occulter S/C, flying in a close proximity (about 150m with accuracy of a few mm) at apogee of a Highly Elliptical Orbit (HEO) 600 x 60 530 km, 59° incl.
- A giant coronagraph is implemented by one satellite occulting the sun and the other satellite flying a telescope

➤ Giant Coronagraph System (ASPIICS):

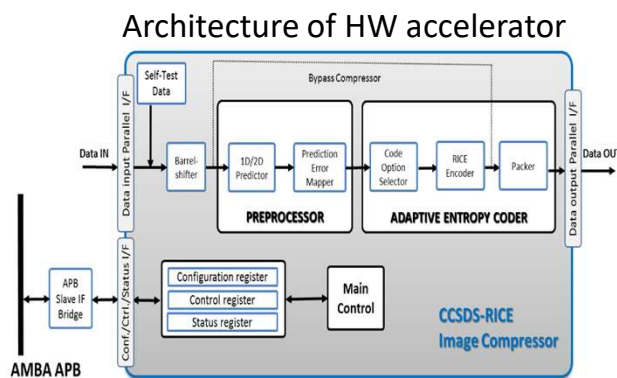
- Will be the first space coronagraph to cover 1.08 and 3 solar radii where the magnetic field plays a crucial role in the coronal dynamics
- Will provide continuous observational conditions very close to total solar eclipse, but without the effects of the Earth's atmosphere
- ASPIICS will provide novel solar observations to achieve the two major solar physics science objectives:
 - Understand physical processes that govern the quiescent solar corona
 - Understand physical processes that lead to CMEs and determine space weather



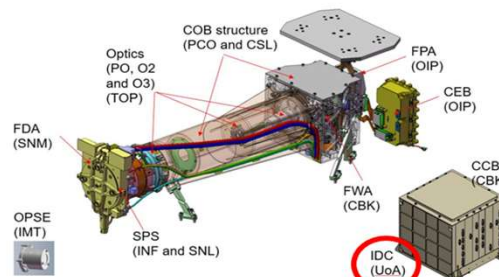
ESA PROBA-3 Giant Coronagraph System (2009-2025)

Image Data Compression Algorithm and HW Accelerator (IP core in FPGA technology)

– Based on CCSDS 121 Lossless Data Compression enhanced for 2D coronagraph images



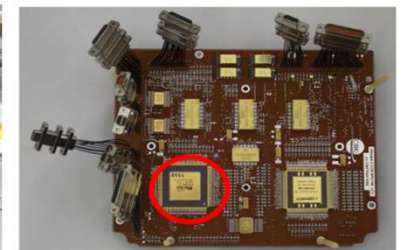
Overview of ASPIICS Coronagraph Instrument



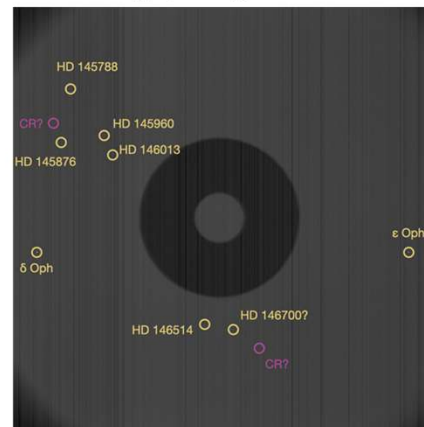
ASPIICS Coronagraph Control Box



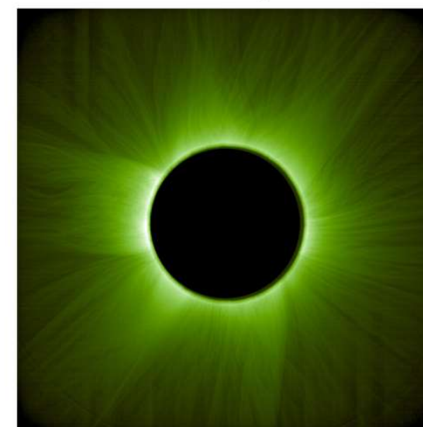
ASPIICS Image Data Compression



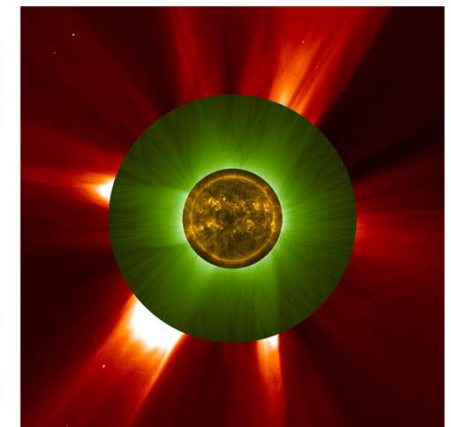
First coronagraph image after IOV



Solar corona viewed by PROBA-3



The Sun and its corona viewed by PROBA-2/3 SOHO



Major Space Upstream Research Projects

➤ EXCELLENCE-II (2014-2015) DSCAL PI

- SCORPIUS-5149, “Single-Chip Radiation Tolerant Dynamically Reconfigurable Payload Data Processing Units for Future Space Applications”

➤ Research>Create-Innovate (2018-2022), DSCAL PI

- SYSYFOS - “High-performance and High-reliability Compression and Management of Hyperspectral Image Data”
- First implementation of CCSDS 122.1 Hyperspectral Compression in the World!

➤ Hellenic Foundation for Research & Innovation (H.F.R.I.) – ELIDEK Postdoctoral Research Grant (2018-2021) DSCAL PI

- “Renata: Next Generation Hardware Accelerated Onboard Hyperspectral Data Handling”
- First implementation of CCSDS 123.0-B2 Hybrid Encoder in the World!

➤ H2020-COMPET-3-2017 (2018-2022): High-speed data chain

- Hi-SIDE: High-Speed Integrated Satellite Data Systems For Leading EU Industry
- Integrated and validated in ABDS-SAS KUP Board in Airbus D&S premises

➤ “CCSDS 123.0-B-2 Lossless/lossy multispectral & hyperspectral compression IP core” ESA Contract No. 4000136723/22/NL/CRS

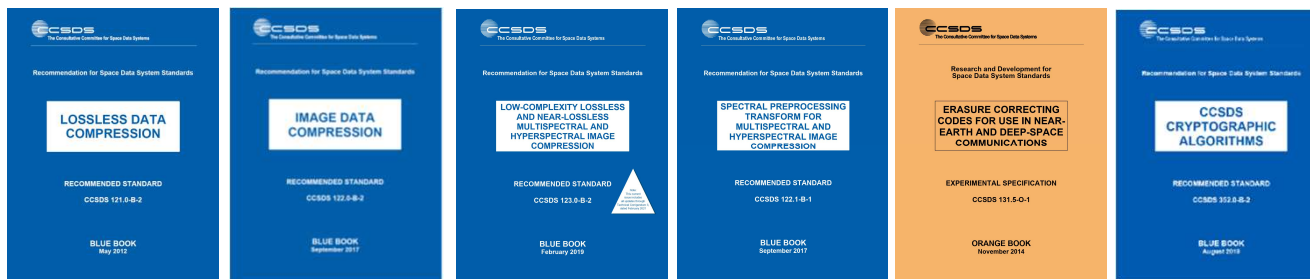
- CCSDS 123.0-B2 Hybrid Encoder, as IP Core, available from ESA for future space missions



Space Upstream Cutting-Edge Technology *Designed in Greece*

➤ Portfolio of State-of-the-art competitive HW accelerators, as IP Cores

- Targeting space-grade (i.e. V5QV, KU060, RTG4) and COTS (i.e. Zynq 7000) FPGAs
 - CCSDS 123.0-B-1/2 Lossless/Near Lossless Multi-/Hyperspectral Image Compression (novel parallel and scalable architecture) (**double performance than ESA IP core, novel SAR compression, flight heritage from ERMIS mission**)
 - CCSDS 122.0-B-1 Image Data Compression (**competitive design, flight heritage from ERMIS mission**)
 - CCSDS 122.1 Transform based Multi-/Hyperspectral Image Compression (**World's first implementation**)
 - CCSDS 121.0-B-2 Lossless Data Compression (**flight heritage from PROBA-3 mission**)
 - CCSDS 131.1-0-2 Low-Density Parity-Check (LDPC) codes (C2, AR4JA) (**best performance**)
 - CCSDS 131.5-0-1 Packet-Level Erasure Coding (**World's first implementation**)
 - CCSDS 142.0-B-2 03K LDPC channel-coding (**much less foot print than ESA IP core, flight heritage from ERMIS mission**)
 - CCSDS 352.0-B-2 Cryptographic Algorithms AES-GCM 256 (**competitive design**)



The **FASTEST** implementations of CCSDS recommended standards for image & data compression in the market

- Can be fine-tuned based on mission-specific requirements
- Fully parallel, deeply pipelined architecture
- Fully configurable using compile-time and runtime configuration
- Easy system integration



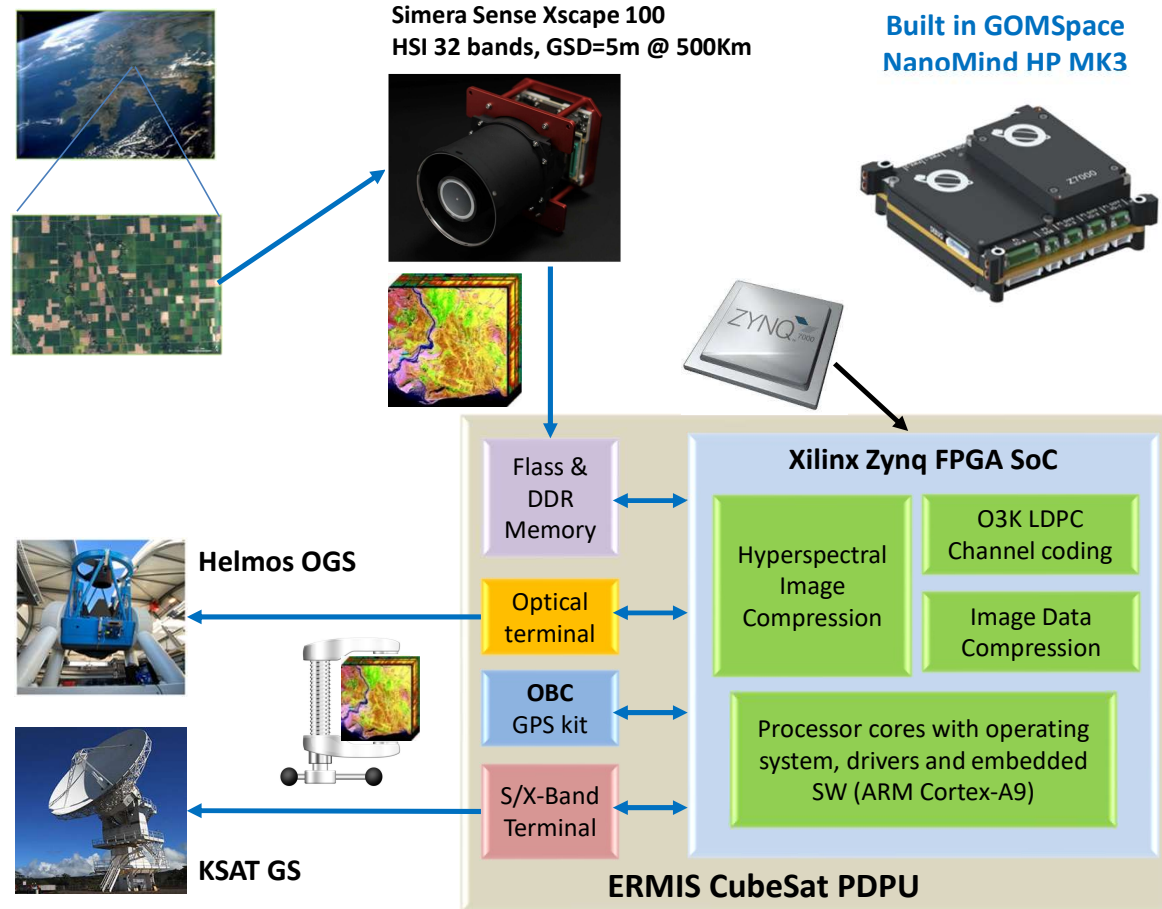
Payload Data Processing Unit for ERMIS Mission *Designed in Greece*

Interfaces

- Data: 100Mbps SpW
- TMTC: CANbus/I²C/RS-422/SpW

Functional description

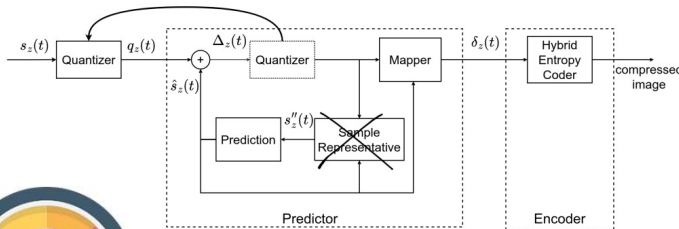
- All modes read from or write to flash (no temporary storage on DRAM)
- Camera readout to flash: control camera interface (CAN/I²C)
- CCSDS 122/123 compression: read from flash-compress-write to flash
- Optical downlink: read compressed data from flash & transmit to terminal with/without CCSDS 142 encoding (on-line)
- S/X band downlink: read compressed data from flash & transmit to terminal
- Different bitstreams: radiation protection
- Controller application (on PS) to handle data flows
- **Flight heritage in Q1/2026 (ERMIS mission)**



CCSDS 123 Lossless/Near Lossless Multispectral & Hyperspectral Image Compression

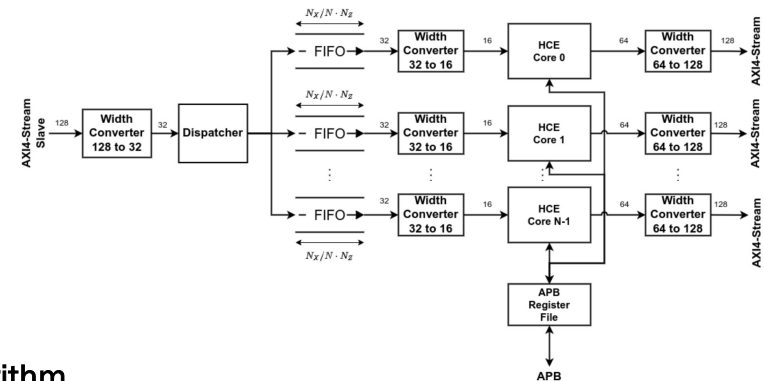
Designed in Greece

➤ CCSDS 123 IP Core: Lossless and Near Lossless Hyperspectral Compression

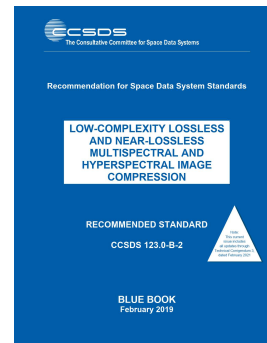


- ✓ **Single Core => 4.56 Gbps @1.67W**
- ✓ **Six Cores => 25.44 Gbps @6.12W**

- Quality limited and prediction-based compression algorithm
- Lossless/Near-lossless compression using pre-quantization and segmentation
 - Novel scalable, parallel & high-throughput compression architecture
 - High power-efficiency (power measured using on-chip SYSMON)
- Integrated in ABDS-SAS KUP Board (H2020 Hi-SIDE Project)
- CCSDS 123.0-B-2 Hybrid Encoder: World's first implementation
 - Part of ESA Contract No. 4000136723/22/NL/CRS CCSDS 123.0-B-2 IP Core
- **Flight heritage in Q1/2026 (ERMIS mission)**

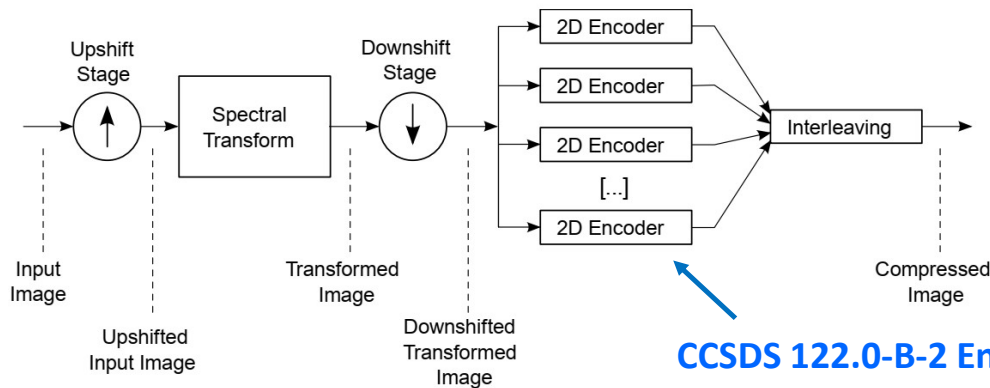


Collaboration with
AIRBUS in the
development of on-
board hyperspectral
image compression
subsystems for next-
generation satellites
(EU Hi-SIDE project)



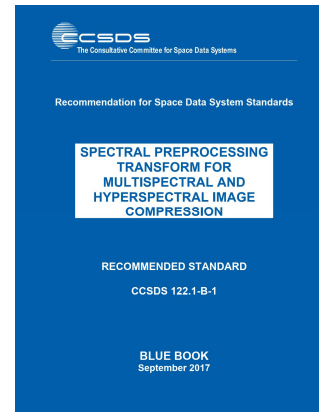
CCSDS 122 Deep Lossy Hyperspectral Image Compression *Designed in Greece*

➤ CCSDS 122 set of IP Cores: Deep Lossy, Rate-Limited Hyperspectral Compression



Collaboration on
high-throughput
compression
schemes

- Rate-limited and transformed-based compression based on CCSDS 122 2D Encoder
- Deep lossy compression (<1.5 bpp) using spectral transform and rate allocation
- Supported spectral transformations in HW:
 - Integer Wavelet Transform (5-stage CDF 5/3, same as JPEG2K)
 - Pairwise Orthogonal Transform (POT) – KLT approximation (under development)
- Rate allocation algorithm in HW: Reverse Water Filling
- **World's first implementation**
- **Flight heritage in Q1/2026 for CCSDS 122.0-B-2 Encoder IP core (ERMIS mission)**

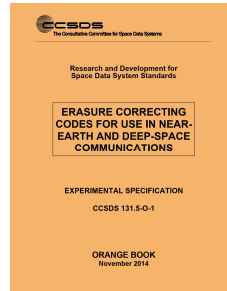
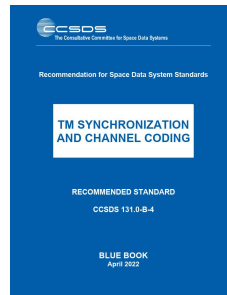
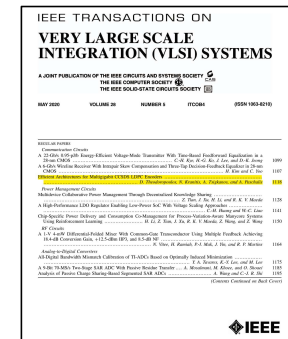


Channel Coding for RF and Optical Terminals *Designed in Greece*

➤ State-of-the-art CCSDS QC LDPC Encoding Architecture and IP core implementation:

- CCSDS 131.0-B-3 TM Channel Coding IP Cores for RF channels
 - Rate 223/255 **C2** code (8160/7136)
 - Near-Earth – High data-rates, small foot-print
 - Nine **AR4JA** codes: rates $\frac{1}{2}$, $\frac{2}{3}$, and $\frac{4}{5}$
block lengths $k=1024, 4096$ and 16384 bits
 - Deep-Space – Very low SNR
- CCSDS 131.5-0-1 Erasure Correcting Codes IP Cores
 - Packet-level encoding algorithms for near-earth and deep space communication
- CCSDS 142.0-B-2 Optical On/Off Keying (OOK) IP Cores for optical links
 - Rate 9/10 Accumulate-Repeat-Accumulate (ARA) LDPC code block length $k=27648$
 - Rate 1/2 Protograph-Based Raptor-Like (PBRL) LDPC code block length $k=15360$
 - Integrated in ERMIS Payload Data Processing Unit (GOMSpace NanoMind HP MK3)
 - Encoded data are directly transferred to ERMIS Optical Terminal modulator (Astrolight ATLAS-1)
 - **Flight heritage in Q1/2026 (ERMIS mission)**

Collaboration on space optical communication providing encoder and decoder FEC schemes



Recent and current collaborations

- Collaboration with **AIRBUS D&S** in the development of **on-board hyperspectral image compression subsystems** for next-generation satellites (EU HORIZON Hi-SIDE project)
 - Innovation in Space Award 2022 at the European Space Forum
- Collaboration with **ISD** and **AIRBUS UK** in the development of the Payload Processing Unit for the TRUTHS mission (ESA institutional mission)
- Collaboration with **ICEYE** in the development of novel **hardware accelerators for SAR compression** to be integrated in their next generation SAR satellites (National Space Program)
- Collaboration with **ISD** in the development of **hardware accelerators for 5G channel coding** for Ship Structural Health Monitoring (EU program)
- Collaboration with **ISD** in the development of novel **hardware accelerators for critical channel-coding** to be integrated in the European RF System-on-Chip for D&S applications (EU program)
- Collaboration with **ISD** in the development of **novel AI-based hardware accelerators for vessel detection** (EU HORIZON NeAIxt project)



Our vision

➤ Center of Excellence in Space Upstream Technology

- ✓ Create Payload Data Processing Units and a Portfolio of State-of-the-art competitive HW accelerators, as IP Cores implemented in space-grade and COTS FPGAs in accordance to Consultative Committee for Space Data Systems (CCSDS) recommended standards
- ✓ Provide the European space supply chain with products and services as Center of Excellence in On-Board Data Subsystems domain

