



dscal
DIGITAL SYSTEMS & COMPUTER ARCHITECTURE LABORATORY

Εργαστήριο Λογικής Σχεδίασης

3^ο Εργαστηριακό Μάθημα

Βασιλόπουλος Διονύσης

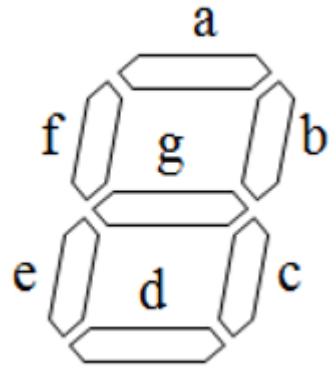
Ε.Δι.Π. Τμήματος Πληροφορικής & Τηλεπικοινωνιών - ΕΚΠΑ

3^η Εργαστηριακή Άσκηση

Δημιουργήστε μία ALU που να προσθέτει δύο μη προσημασμένους αριθμούς ($a+b$) ή να διπλασιάζει έναν μη προσημασμένο αριθμό (a). Οι αριθμοί a, b είναι των 3 bit ενώ το αποτέλεσμα και των δύο πράξεων αποθηκεύεται στο σήμα Result των 4 bit. Εμφανίστε το αποτέλεσμα τόσο στα LED όσο και στο Pmod. Για την είσοδο των αριθμών a, b όσο και για την επιλογή της πράξης θα χρησιμοποιήσετε τα SW της κάρτας.

3^η Εργαστηριακή Άσκηση

VHDL – 7 segment led



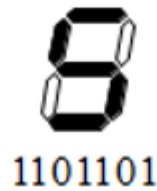
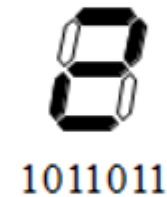
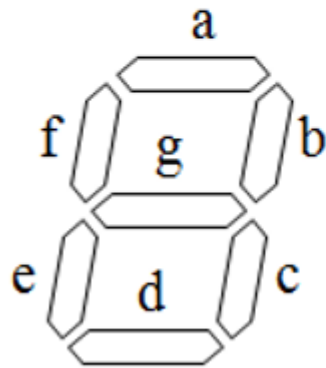
Αναπαράσταση με 7-bit
MSB->g - LSB->a

g-f-e-d-c-b-a

3^η Εργαστηριακή Άσκηση

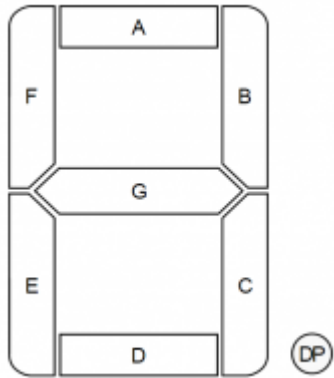
VHDL – 7 segment led

– Τμήματα: (g, f, e, d, c, b, a)



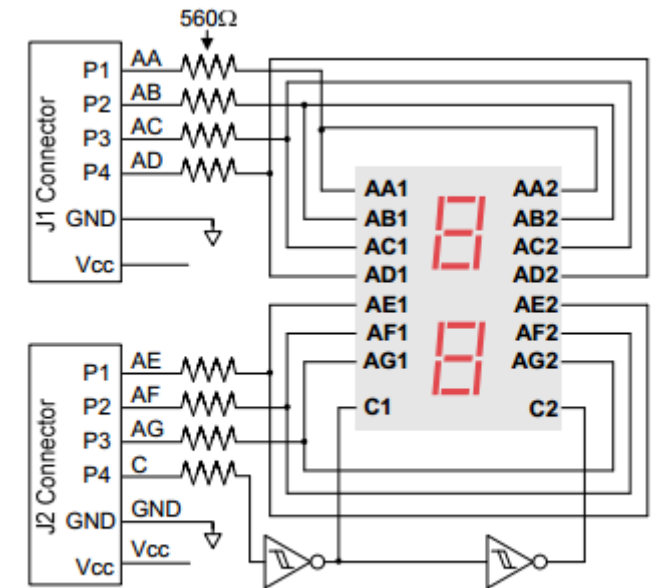
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7 segment led - Pmod



Pinout Description Table

Header J1			Header J2		
Pin	Signal	Description	Pin	Signal	Description
1	AA	Segment A	1	AE	Segment E
2	AB	Segment B	2	AF	Segment F
3	AC	Segment C	3	AG	Segment G
4	AD	Segment D	4	C	Digit Selection pin
5	<u>GND</u>	Power Supply Ground	5	<u>GND</u>	Power Supply Ground
6	<u>VCC</u>	Positive Power Supply	6	<u>VCC</u>	Positive Power Supply



Seven-Segment Display Connection Diagram

ΜΟΝΟ ΤΟ ΈΝΑ ΑΠΌ ΤΑ 2 LED ΜΠΟΡΕΙ ΝΑ ΕΊΝΑΙ ΑΝΑΜΕΝΟ ΣΕ ΚΆΘΕ ΧΡΟΝΙΚΗ ΣΤΙΓΜΗ

Pmod: Peripheral Module interface

Εικόνες από το <https://reference.digilentinc.com/reference/pmod/pmodssd/reference-manual>

3^η Εργαστηριακή Άσκηση

7 segment led - Pmod

Table 16 - Pmod Connections

Pmod	Signal Name	Zynq pin	Pmod	Signal Name	Zynq pin
JA1	JA1	Y11	JB1	JB1	W12
	JA2	AA11		JB2	W11
	JA3	Y10		JB3	V10
	JA4	AA9		JB4	W8
	JA7	AB11		JB7	V12
	JA8	AB10		JB8	W10
	JA9	AB9		JB9	V9
	JA10	AA8		JB10	V8

Θα βρείτε σε ποια Signal της FPGA αντιστοιχούν τα signal του Pmod.
Κατόπιν θα βρείτε σε ποια pin της FPGA αντιστοιχούν τα signal του Pmod.

3^η Εργαστηριακή Άσκηση

ΠΡΟΧΩΡΗΣΤΕ ΣΤΗΝ ΑΣΚΗΣΗ



3^η Εργαστηριακή Άσκηση

Αρχιτεκτονική

```
result_temp<=unsigned('0'&a)+ unsigned('0'&b) when ctr='1' else  
    unsigned(a&'0') when ctr='0' else  
    (others=>'0');
```

Αρχιτεκτονική



```
result<=std_logic_vector(result_temp);
```

```
with result_temp select  
seven_segment<="0111111" when "0000", --0  
    "0000110" when "0001", --1  
    "1011011" when "0010", --2  
    "1001111" when "0011", --3  
    "1100110" when "0100", --4  
    "1101101" when "0101", --5  
    "1111101" when "0110", --6  
    "0000111" when "0111", --7  
    "1111111" when "1000", --8  
    "1101111" when "1001", --9  
    "1000000" when others;
```

```
digit_selection_out<=digit_selection_in;
```


3^η Εργαστηριακή Άσκηση

Constraints (1/2) – Switches + Leds

```
# ZedBoard Pin Assignments
#####
# On-board Slide Switches #
#####

set_property -dict { PACKAGE_PIN M15  IOSTANDARD LVCMOS33 } [get_ports { digit_selection_in }];
set_property -dict { PACKAGE_PIN H19  IOSTANDARD LVCMOS33 } [get_ports { ctr }];
set_property -dict { PACKAGE_PIN F21  IOSTANDARD LVCMOS33 } [get_ports { b[1] }];
set_property -dict { PACKAGE_PIN H22  IOSTANDARD LVCMOS33 } [get_ports { b[0] }];
set_property -dict { PACKAGE_PIN G22  IOSTANDARD LVCMOS33 } [get_ports { a[1] }];
set_property -dict { PACKAGE_PIN F22  IOSTANDARD LVCMOS33 } [get_ports { a[0] }];

#####
# On-board Leds #
#####

set_property -dict { PACKAGE_PIN T22  IOSTANDARD LVCMOS33 } [get_ports { result[0] }];
set_property -dict { PACKAGE_PIN T21  IOSTANDARD LVCMOS33 } [get_ports { result[1] }];
set_property -dict { PACKAGE_PIN U22  IOSTANDARD LVCMOS33 } [get_ports { result[2] }];
```

Constraints



3^η Εργαστηριακή Άσκηση

Constraints (1/2) – Pmod

```
#####  
# PmodSSO                #  
#####
```

```
set_property -dict { PACKAGE_PIN Y11  IOSTANDARD LVCMOS33 } [get_ports { seven_segment[0] }];  
set_property -dict { PACKAGE_PIN AA11 IOSTANDARD LVCMOS33 } [get_ports { seven_segment[1] }];  
set_property -dict { PACKAGE_PIN Y10  IOSTANDARD LVCMOS33 } [get_ports { seven_segment[2] }];  
set_property -dict { PACKAGE_PIN AA9  IOSTANDARD LVCMOS33 } [get_ports { seven_segment[3] }];  
set_property -dict { PACKAGE_PIN W12  IOSTANDARD LVCMOS33 } [get_ports { seven_segment[4] }];  
set_property -dict { PACKAGE_PIN W11  IOSTANDARD LVCMOS33 } [get_ports { seven_segment[5] }];  
set_property -dict { PACKAGE_PIN V10  IOSTANDARD LVCMOS33 } [get_ports { seven_segment[6] }];  
  
set_property -dict { PACKAGE_PIN W8  IOSTANDARD LVCMOS33 } [get_ports { digit_selection_out }];
```

Constraints



3^η Εργαστηριακή Άσκηση

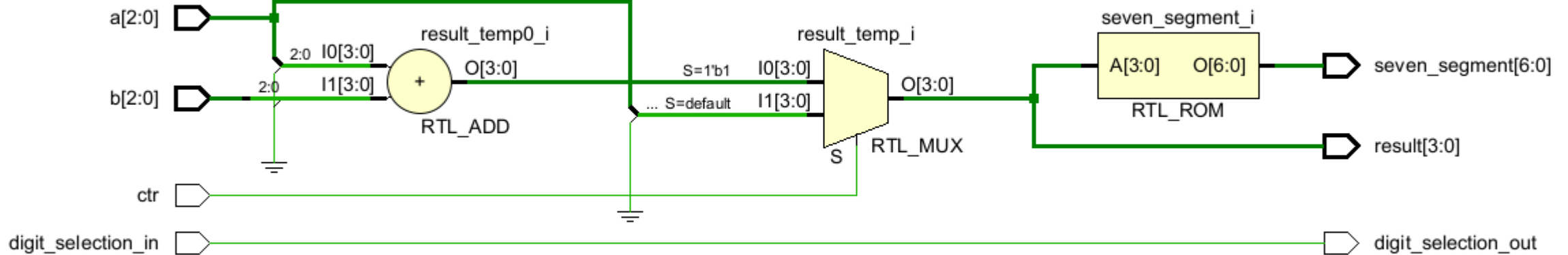
Pmod Manual

Manual Pmod

<https://reference.digilentinc.com/reference/pmod/pmodssd/reference-manual>

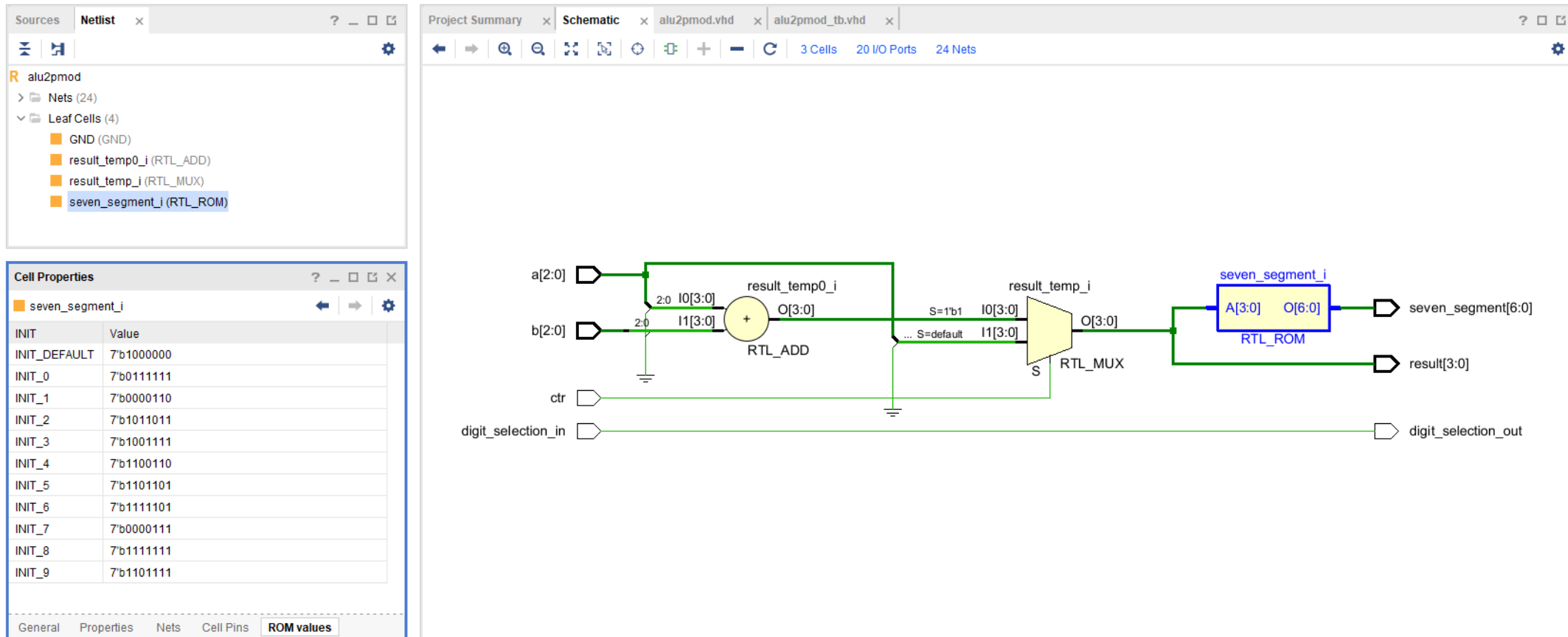
3^η Εργαστηριακή Άσκηση

RTL Design



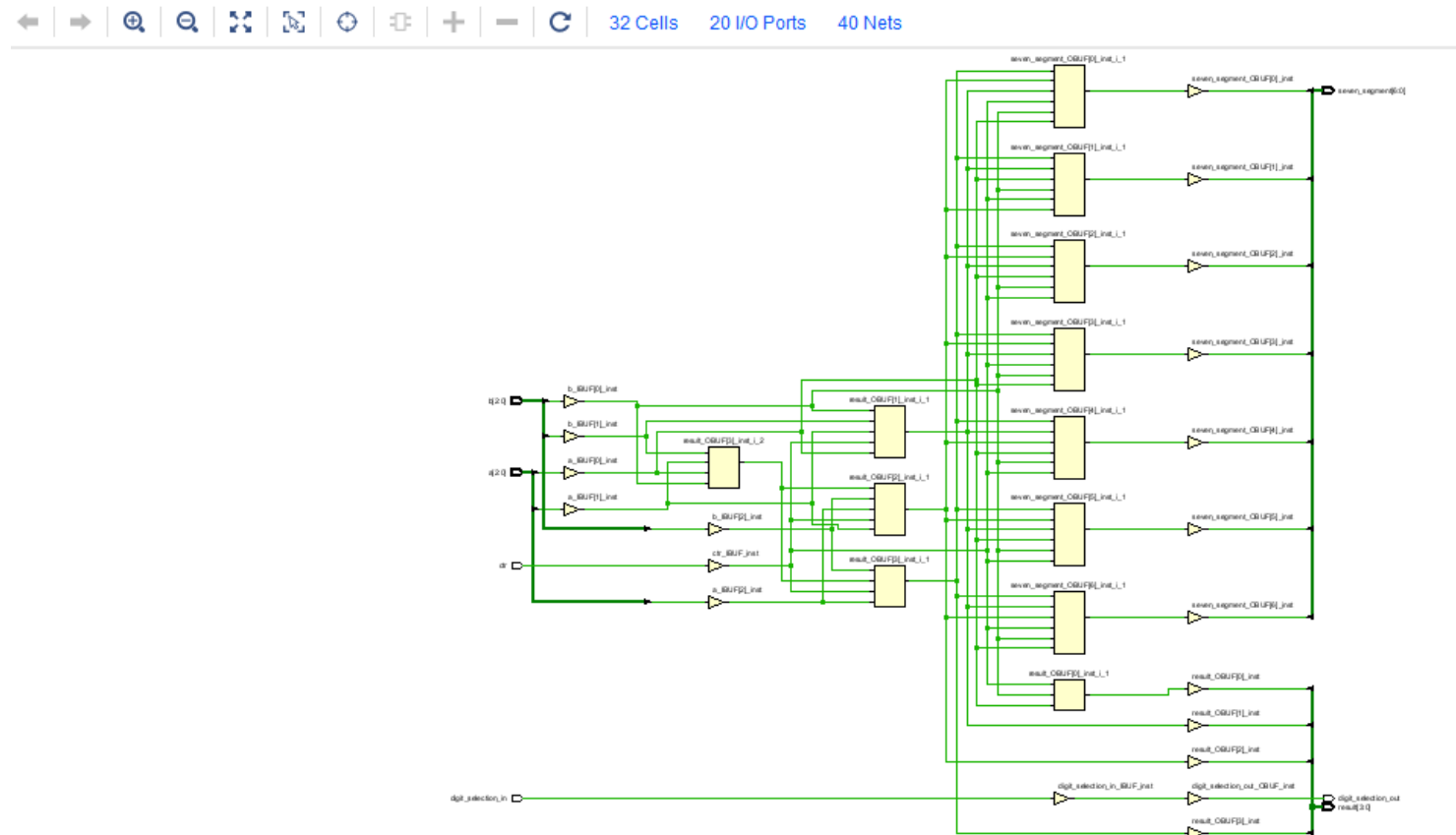
3^η Εργαστηριακή Άσκηση

RTL Design – ROM Module/ROM Values



3^η Εργαστηριακή Άσκηση

Synthesis/Implementation – Schematic



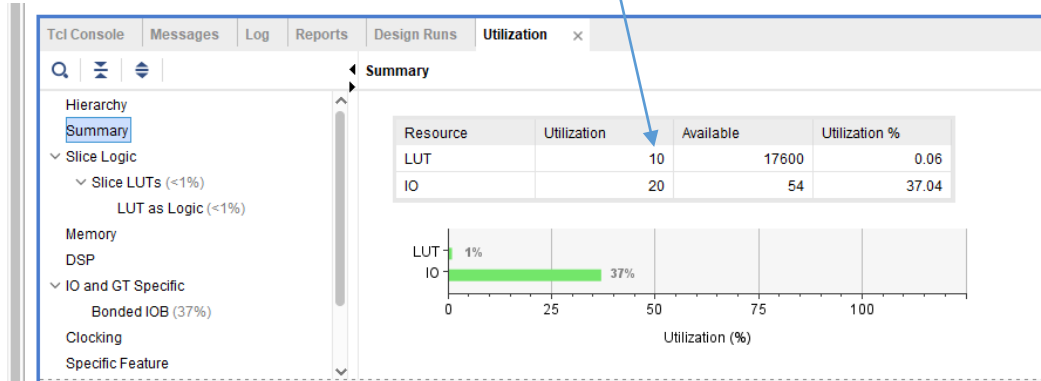
3^η Εργαστηριακή Άσκηση

Implementation – Report Utilization (1/3)

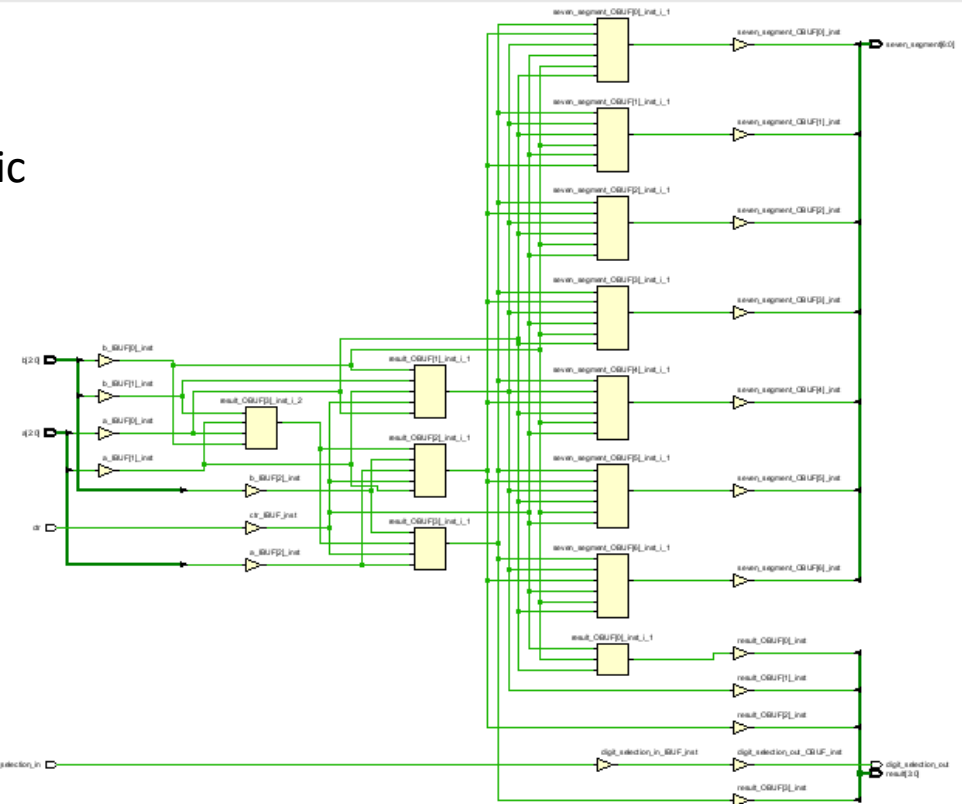
Και από Project Summary

Λιγότερα LUT από όσα δείχνει το schematic
Κάποια συγχωνεύονται (paired), κάποια παραμένουν (placed)

- Report DRC
- Report Noise
- Report Utilization**
- Report Power
- Schematic
- IMPLEMENTATION
 - Run Implementation
 - Open Implemented Design
- PROGRAM AND DEBUG
 - Generate Bitstream



32 Cells 20 I/O Ports 40 Nets



3^η Εργαστηριακή Άσκηση

Implementation – Report Utilization (2/3)

The screenshot displays the Xilinx Vivado implementation report for a design named 'xc7z010iclg225-1L'. The interface is divided into several panes:

- Netlist:** Lists the implemented components, including seven-segment display drivers (seven_segment_OBUF) and LUTs (LUT6).
- Cell Properties:** Shows the properties for the selected cell 'result_OBUF[0]_inst_i_1'. The 'STATUS' field is highlighted in red and labeled 'PLACED', indicating that the cell has been successfully placed in the target device.
- Schematic:** Displays the circuit diagram, showing the interconnections between the LUTs and OBUFs. The connections are shown in green, and the components are represented by yellow blocks.

PRIMITIVE_GROUP	LUT
PRIMITIVE_LEVEL	LEAF
PRIMITIVE_SUBGROUP	others
PRIMITIVE_TYPE	LUT.others.LUT3
REF_NAME	LUT3
REUSE_STATUS	
SLR_INDEX	0
STATUS	PLACED

3^η Εργαστηριακή Άσκηση

Implementation – Report Utilization (3/3)

IMPLEMENTED DESIGN - xc7z010iclg225-1L

Sources Netlist

- result_OBUF[2]_inst (OBUF)
- result_OBUF[2]_inst_i_1 (LUT5)
- result_OBUF[3]_inst (OBUF)
- result_OBUF[3]_inst_i_1 (LUT4)
- result_OBUF[3]_inst_i_2 (LUT4)
- seven_segment_OBUF[0]_inst (OBUF)
- seven_segment_OBUF[0]_inst_i_1 (LUT6)
- seven_segment_OBUF[1]_inst (OBUF)
- seven_segment_OBUF[1]_inst_i_1 (LUT6)

Cell Properties

result_OBUF[2]_inst_i_1

PRIMITIVE_LEVEL	LEAF
PRIMITIVE_SUBGROUP	others
PRIMITIVE_TYPE	LUT.others.LUT5
REF_NAME	LUT5
REUSE_STATUS	
SLR_INDEX	0
SOFT_HLUTNM	soft_lutpair0
STATUS	PLACED

Project Summary | Device | alu2pmod.vhd | alu2pmod_tb.vhd | Schematic

32 Cells | 20 I/O Ports | 40 Nets

The schematic diagram shows a complex logic circuit. On the left, there are several input buffers labeled 'b_BUF[0]_inst' through 'b_BUF[4]_inst'. These are connected to a central logic block containing several LUTs (LUT5 and LUT4) and OBUFs (OBUF2 and OBUF3). The outputs of these LUTs are connected to a series of OBUFs on the right, which are then connected to external pins. A blue box highlights a specific LUT5 cell, and a red circle highlights the 'soft_lutpair0' property in the Cell Properties window. A blue arrow points from the red circle to the highlighted LUT5 cell in the schematic.

3^η Εργαστηριακή Άσκηση

Implementation – Timing Reports (1/2)

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Logic %	Net %	Requirement	Source Clock	Destination Clock	Exception	Skew	Clot
Unconstrained Paths (1)																	
(none) (10)																	
Path 11	∞ ns	5	4	8	a[1]	seven_segment[6]	9.472	4.203	5.269	44.4	55.6	∞	input port clock				
Path 12	∞ ns	5	4	8	a[1]	seven_segment[4]	9.311	4.191	5.120	45.0	55.0	∞	input port clock				
Path 13	∞ ns	5	4	8	a[1]	seven_segment[5]	9.083	4.185	4.898	46.1	53.9	∞	input port clock				
Path 14	∞ ns	5	4	8	a[1]	seven_segment[3]	9.009	4.198	4.811	46.6	53.4	∞	input port clock				
Path 15	∞ ns	5	4	8	a[1]	seven segment[2]	8.989	4.181	4.809	46.5	53.5	∞	input port clock				

Menu Reports->Timing-Timing Reports

Setup Time:

Αναφέρεται στις αργές διαδρομές (καθυστέρηση διάδοσης)

Τα μονοπάτια (path) με τους χρόνους

3^η Εργαστηριακή Άσκηση

Implementation – Timing Reports (2/2)

The screenshot displays the Vivado IDE interface. The top window shows a schematic diagram of a circuit with various logic blocks and interconnections. The bottom window shows the 'Timing Checks - Hold' report, which is a table listing timing paths and their characteristics.

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Logic %	Net %	Requirement	Source Clock	Destination Clock	Exception
Unconstrained Paths (1)															
(none) (10)															
Path 1	∞ ns	2	1	1	digit_selection_in	digit_selection_out	1.912	1.377	0.535	72.0	28.0	-∞	input port clock		
Path 2	∞ ns	3	2	10	b[0]	seven_segment[2]	2.254	1.390	0.864	61.7	38.3	-∞	input port clock		
Path 3	∞ ns	3	2	10	b[0]	seven_segment[3]	2.275	1.407	0.868	61.8	38.2	-∞	input port clock		
Path 4	∞ ns	3	2	11	ctr	seven_segment[0]	2.298	1.487	0.812	64.7	35.3	-∞	input port clock		
Path 5	∞ ns	3	2	11	ctr	seven segment[1]	2.303	1.486	0.817	64.5	35.5	-∞	input port clock		

Hold Time:

Αναφέρεται στις γρήγορες διαδρομές (καθυστέρηση μόλυνσης)

Τα μονοπάτια (path) με τους χρόνους

3^η Εργαστηριακή Άσκηση

Implementation – Path Analysis

The screenshot displays the Path Analysis tool in Vivado. The main window shows the 'Data Path' table for Path 11, which details the delay components from source to destination. The 'Data Path' table is as follows:

Delay Type	Incr (ns)	Path (ns)	Location	Netlist Resource(s)
net (fo=0)	(r) 0.000	0.000	Site: P10	a[1]
IBUF (Prop.obuf I O)	(r) 0.966	0.966	Site: P10	a_IBUF[1]_instI
net (fo=3, routed)	1.589	2.556		a_IBUF[1]
LUT4 (Prop.t4_11 O)	(r) 0.124	2.680	Site: SLICE_X43Y7	result_OBUF[3]_inst_i_2I1
net (fo=2, routed)	0.433	3.112		result_OBUF[3]_inst_i_2_n_0
LUT4 (Prop.t4_11 O)	(r) 0.150	3.262	Site: SLICE_X43Y7	result_OBUF[3]_inst_i_1I1
net (fo=8, routed)	1.575	4.837		result_OBUF[3]
LUT6 (Prop.t6_10 O)	(r) 0.326	5.163	Site: SL...E_X43Y14	seven_segment_OBUF[6]_inst_i_1I0
net (fo=1, routed)	1.672	6.836	Site: SL...E_X43Y14	seven_segment_OBUF[6]_inst_i_1I0
net (fo=0)	(r) 2.637	9.472	Site: R13	seven_segment_OBUF[6]_instI
net (fo=0)	0.000	9.472	Site: R13	seven_segment_OBUF[6]_instI0
net (fo=0)			Site: R13	seven_segment[6]

The 'Timing Checks - Setup' table at the bottom provides a summary of the path analysis:

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Logic %	Net %	Requirement	Source Clock	Destination Clock	Exception	Skew	Clock	
Unconstrained Paths (1)																		
(none) (10)																		
Path 11	∞	5	4	8	a[1]	seven_segment[6]	9.472	4.203	5.269	44.4	55.6	∞	input port clock					

Δεξί κλικ στο Path και
[View Path Report](#)

3^η Εργαστηριακή Άσκηση

Implementation – Simulation

```
test_1: process is
begin
ctr_tb<= not ctr_tb;
for i in 0 to 3 loop
    a_tb<=std_logic_vector(to_unsigned(i,a_tb'length));
    for j in 0 to 3 loop
        b_tb<=std_logic_vector(to_unsigned(j,a_tb'length));
        wait for 10ns;
    end loop;
end loop;
end process test_1;
```