

Εργαστήριο Space Data Systems

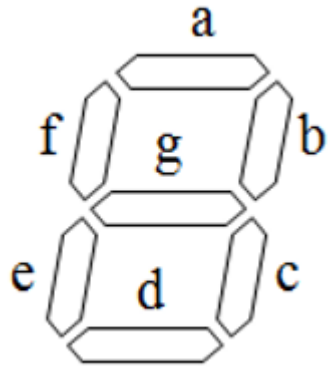
2^ο Εργαστηριακό Μάθημα

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2^η Εργαστηριακή Άσκηση

VHDL – 7 segment led



Αναπαράσταση με 7-bit
MSB->g - LSB->a

g-f-e-d-c-b-a

2^η Εργαστηριακή Άσκηση

VHDL – 7 segment led

- Κώδικας BCD: Δυαδικά κωδικοποιημένοι δεκαδικοί
 - Κώδικας 4 bit για τα δεκαδικά ψηφία

0: 0000	1: 0001	2: 0010	3: 0011	4: 0100
5: 0101	6: 0110	7: 0111	8: 1000	9: 1001

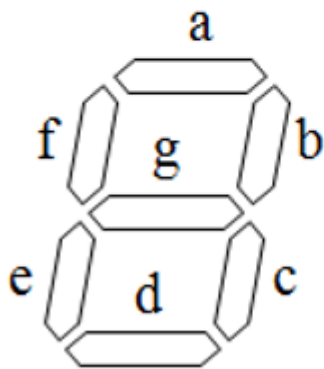
Υπάρχουν και άλλες δυνατές αναπαραστάσεις;











Υπάρχει πλεονασμός στη χρήση των bit;

2^η Εργαστηριακή Άσκηση

VHDL – 7 segment led

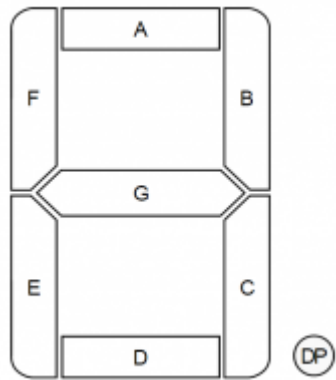
- Αποκωδικοποιεί τον κώδικα BCD (binary coded decimal) για να οδηγήσει μια οθόνη (LED ή LCD) 7 τμημάτων
 - Τμήματα: (g, f, e, d, c, b, a)



				
0111111	0000110	1011011	1001111	1100110
				
1101101	1111101	0000111	1111111	1101111

2^η Εργαστηριακή Άσκηση

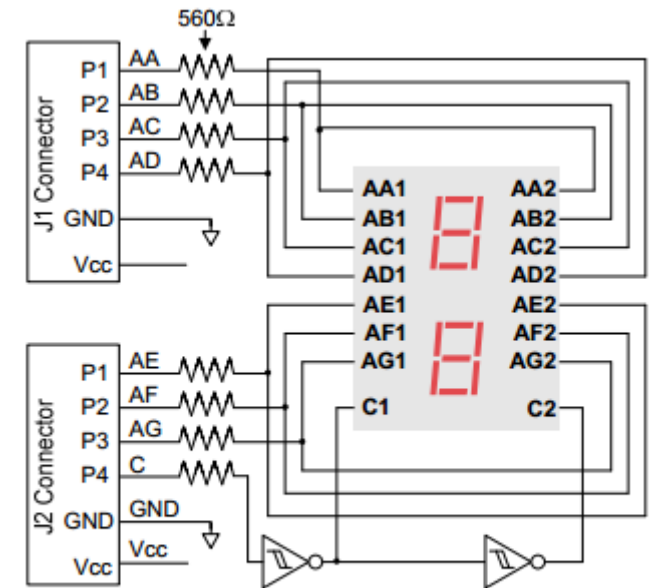
7 segment led - Pmod



Pinout Description Table

Header J1			Header J2		
Pin	Signal	Description	Pin	Signal	Description
1	AA	Segment A	1	AE	Segment E
2	AB	Segment B	2	AF	Segment F
3	AC	Segment C	3	AG	Segment G
4	AD	Segment D	4	C	Digit Selection pin
5	GND	Power Supply Ground	5	GND	Power Supply Ground
6	VCC	Positive Power Supply	6	VCC	Positive Power Supply

Pmod



Seven-Segment Display Connection Diagram

ΜΟΝΟ ΤΟ ΈΝΑ ΑΠΌ ΤΑ 2 LED ΜΠΟΡΕΙ ΝΑ ΕΊΝΑΙ ΑΝΑΜΕΝΟ ΣΕ ΚΆΘΕ ΧΡΟΝΙΚΗ ΣΤΙΓΜΗ

Pmod: Peripheral Module interface

Εικόνες από το <https://reference.digilentinc.com/reference/pmod/pmodssd/reference-manual>

2^η Εργαστηριακή Άσκηση

7 segment led - Pmod

Table 16 - Pmod Connections

Pmod	Signal Name	Zynq pin	Pmod	Signal Name	Zynq pin
JA1	JA1	Y11	JB1	JB1	W12
	JA2	AA11		JB2	W11
	JA3	Y10		JB3	V10
	JA4	AA9		JB4	W8
	JA7	AB11		JB7	V12
	JA8	AB10		JB8	W10
	JA9	AB9		JB9	V9
	JA10	AA8		JB10	V8

Θα βρείτε σε ποια Signal της FPGA αντιστοιχούν τα signal του Pmod.
Κατόπιν θα βρείτε σε ποια pin της FPGA αντιστοιχούν τα signal του Pmod.

VHDL – Basics – BCD

ΠΡΟΧΩΡΗΣΤΕ ΣΤΗΝ ΑΣΚΗΣΗ



2^η Εργαστηριακή Άσκηση

Αρχιτεκτονική

Αρχιτεκτονική

```
bcd_values: process is
begin
case bcd is
  when X"0" => seven_segment <="0111111"; -- 0
  when X"1" => seven_segment <="0000110"; -- 1
  when X"2" => seven_segment <="1011011"; -- 2
  when X"3" => seven_segment <="1001111"; -- 3
  when X"4" => seven_segment <="1100110"; -- 4
  when X"5" => seven_segment <="1101101"; -- 5
  when X"6" => seven_segment <="1111101"; -- 6
  when X"7" => seven_segment <="0000111"; -- 7
  when X"8" => seven_segment <="1111111"; -- 8
  when X"9" => seven_segment <="1101111"; -- 9
  when others => seven_segment <="1000000"; -- -
end case;
end process bcd_values;
digit_selection_out <=digit_selection_in;
```


2^η Εργαστηριακή Άσκηση

Αρχιτεκτονική

Constraints

```
# On-board Slide Switches #
#####
set_property -dict { PACKAGE_PIN F21 IOSTANDARD LVCMOS33 } [get_ports { bcd[3] }];
set_property -dict { PACKAGE_PIN H22 IOSTANDARD LVCMOS33 } [get_ports { bcd[2] }];
set_property -dict { PACKAGE_PIN G22 IOSTANDARD LVCMOS33 } [get_ports { bcd[1] }];
set_property -dict { PACKAGE_PIN F22 IOSTANDARD LVCMOS33 } [get_ports { bcd[0] }];
set_property -dict { PACKAGE_PIN H19 IOSTANDARD LVCMOS33 } [get_ports { digit_selection_in }];

# On-board led      #
#####
set_property -dict { PACKAGE_PIN Y11 IOSTANDARD LVCMOS33 } [get_ports { seven_segment[0] }];
set_property -dict { PACKAGE_PIN AA11 IOSTANDARD LVCMOS33 } [get_ports { seven_segment[1] }];
set_property -dict { PACKAGE_PIN Y10 IOSTANDARD LVCMOS33 } [get_ports { seven_segment[2] }];
set_property -dict { PACKAGE_PIN AA9 IOSTANDARD LVCMOS33 } [get_ports { seven_segment[3] }];
set_property -dict { PACKAGE_PIN W12 IOSTANDARD LVCMOS33 } [get_ports { seven_segment[4] }];
set_property -dict { PACKAGE_PIN W11 IOSTANDARD LVCMOS33 } [get_ports { seven_segment[5] }];
set_property -dict { PACKAGE_PIN V10 IOSTANDARD LVCMOS33 } [get_ports { seven_segment[6] }];

set_property -dict { PACKAGE_PIN W8 IOSTANDARD LVCMOS33 } [get_ports { digit_selection_out }];
```

2^η Εργαστηριακή Άσκηση

Pmod Manual

Manual LED

<https://reference.digilentinc.com/reference/pmod/pmodssd/reference-manual>

2^η Εργαστηριακή Άσκηση

RTL Design - ROM Module/ROM Values

The screenshot displays the RTL design environment for a ROM module. The left pane shows the Netlist and Cell Properties for the module 'seven_segment_i (RTL_ROM)'. The right pane shows the Schematic diagram with inputs 'digit_selection_in', 'bcd[3:0]', and 'seven_segment_i', and outputs 'digit_selection_out' and 'seven_segmen[6:0]'. The ROM module is highlighted in yellow.

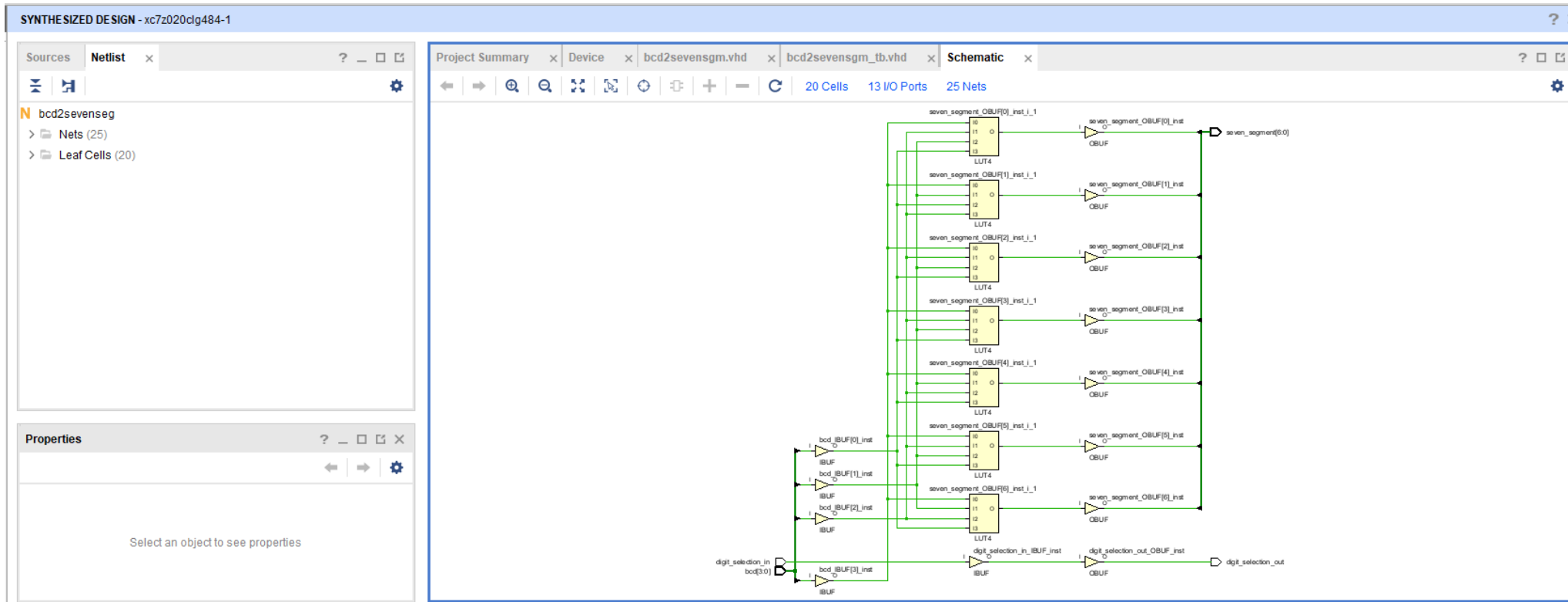
Cell Properties

INIT	Value
INIT_DEFAULT	7'b1000000
INIT_0	7'b0111111
INIT_1	7'b0000110
INIT_2	7'b1011011
INIT_3	7'b1001111
INIT_4	7'b1100110
INIT_5	7'b1101101
INIT_6	7'b1111101
INIT_7	7'b0000111
INIT_8	7'b1111111
INIT_9	7'b1101111

ROM values

2^η Εργαστηριακή Άσκηση

Synthesis/Implementation – Schematic

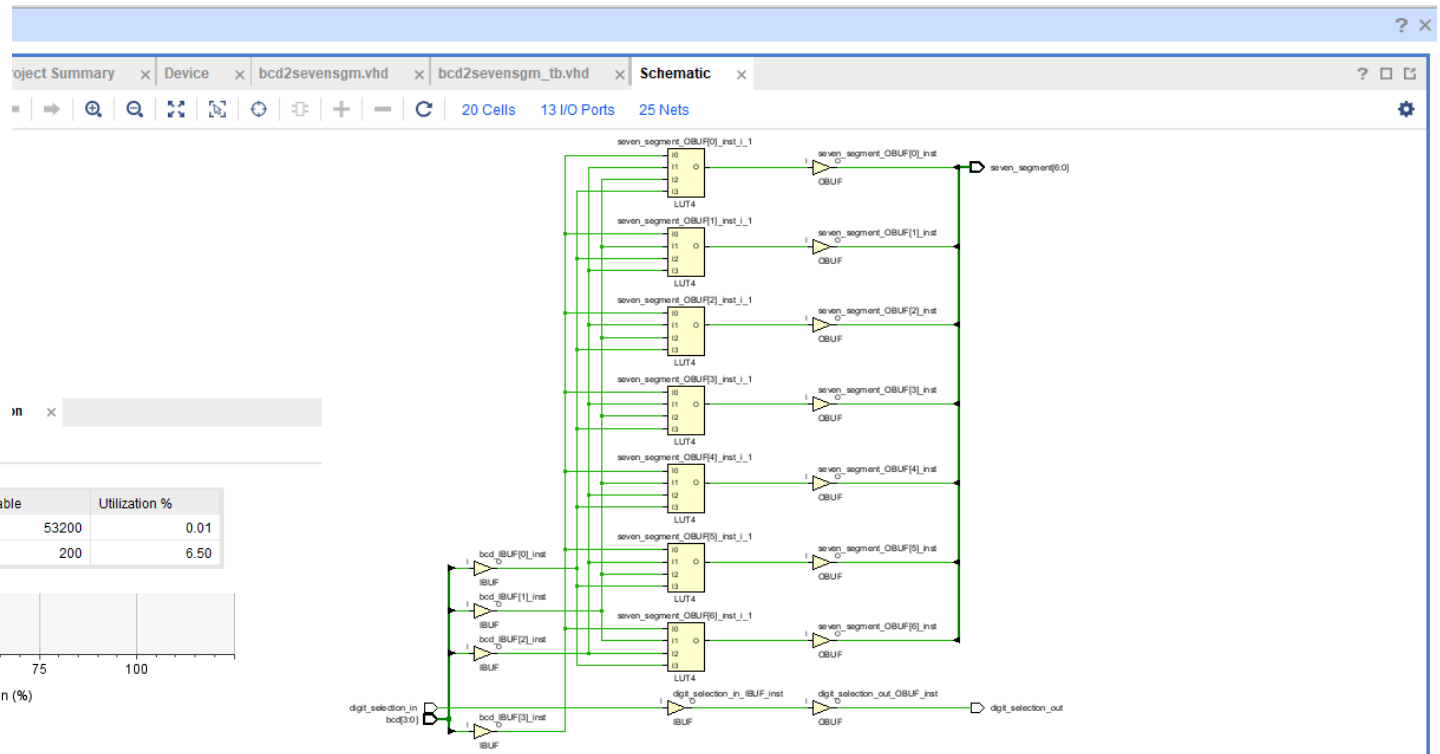


2^η Εργαστηριακή Άσκηση

Implementation – Report Utilization (1/3)

Και από Project Summary

Διαφορετικά Lut στο report από το Design (4 αντί για 7). Κάποια συνενώνονται στο τελικό αποτέλεσμα σχηματίζοντας ζεύγη.



2^η Εργαστηριακή Άσκηση

Implementation – Report Utilization (2/3)

The screenshot displays the Xilinx Vivado implementation report. The Netlist window on the left lists the components used in the design, including seven segment OBUFs and LUT4s. The Cell Properties window shows the details for the selected component, seven_segment_OBUF[6]_inst_i_1, which is a LUT4 and has a status of PLACED. The Schematic window shows the circuit diagram, which includes seven segment OBUFs and LUT4s connected to a digit selection input and output.

Netlist

- seven_segment_OBUF[1]_inst (OBUF)
- seven_segment_OBUF[1]_inst_i_1 (LUT4)
- seven_segment_OBUF[2]_inst (OBUF)
- seven_segment_OBUF[2]_inst_i_1 (LUT4)
- seven_segment_OBUF[3]_inst (OBUF)
- seven_segment_OBUF[3]_inst_i_1 (LUT4)
- seven_segment_OBUF[4]_inst (OBUF)
- seven_segment_OBUF[4]_inst_i_1 (LUT4)
- seven_segment_OBUF[5]_inst (OBUF)
- seven_segment_OBUF[5]_inst_i_1 (LUT4)
- seven_segment_OBUF[6]_inst (OBUF)
- seven_segment_OBUF[6]_inst_i_1 (LUT4)

Cell Properties

PRIMITIVE_LEVEL	LEAF
PRIMITIVE_SUBGROUP	others
PRIMITIVE_TYPE	LUT.others.LUT4
REF_NAME	LUT4
REUSE_STATUS	
SLR_INDEX	0
STATUS	PLACED

Schematic

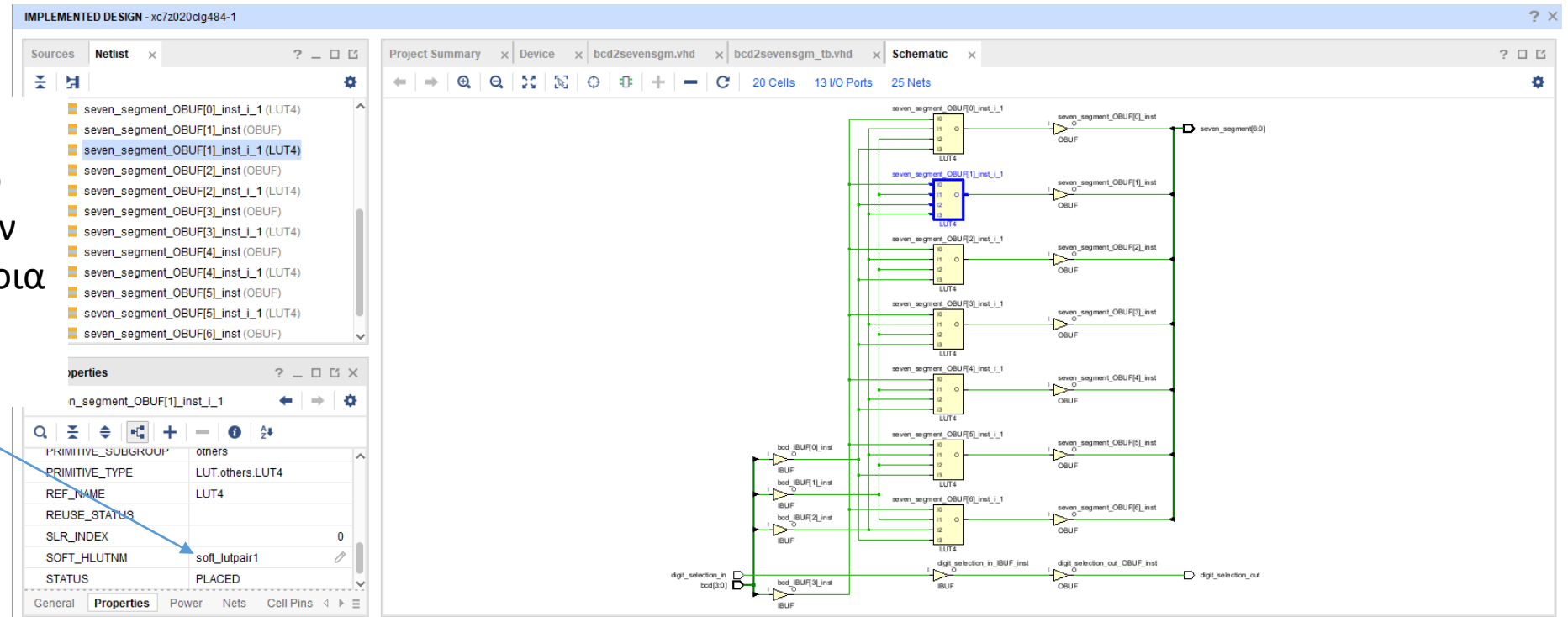
20 Cells 13 I/O Ports 25 Nets

To Lut διατηρείται

2^η Εργαστηριακή Άσκηση

Implementation – Report Utilization (3/3)

Το Lut συνενώνεται με άλλο ένα ώστε να δημιουργήσουν το lutpair1 (υπάρχουν 3 τέτοια ζευγάρια)



2^η Εργαστηριακή Άσκηση

Implementation – Timing Reports (1/2)

The screenshot displays the Xilinx Vivado IDE. The top window shows a schematic of a 7-segment display driver circuit. The bottom window shows the Timing Reports tool, specifically the Setup Checks - Setup section. The table below lists the timing paths and their characteristics.

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Logic %	Net %	Requirement	Source Clock	Destination Clock	Exception
Unconstrained Paths (1)															
(none) (8)															
Path 9	∞	3	2	7	bcd[3]	seven_segment[2]	14.432	5.453	8.979	37.8	62.2	∞	input port clock		
Path 10	∞	3	2	7	bcd[3]	seven_segment[5]	14.246	5.540	8.706	38.9	61.1	∞	input port clock		
Path 11	∞	3	2	7	bcd[3]	seven_segment[3]	14.157	5.206	8.952	36.8	63.2	∞	input port clock		
Path 12	∞	3	2	7	bcd[0]	seven_segment[0]	14.110	5.449	8.661	38.6	61.4	∞	input port clock		
Path 13	∞	3	2	7	bcd[3]	seven_segment[1]	14.018	5.244	8.775	37.4	62.6	∞	input port clock		
Path 14	∞	3	2	7	bcd[0]	seven_segment[4]	13.724	5.337	8.387	38.9	61.1	∞	input port clock		
Path 15	∞	3	2	7	bcd[3]	seven_segment[6]	13.194	5.182	8.012	39.3	60.7	∞	input port clock		
Path 16	∞	2	1	1	digit_selection_in	digit_selection_out	11.422	5.071	6.350	44.4	55.6	∞	input port clock		

Menu Reports->Timing->Report Timing

Setup Time:

Αναφέρεται στις αργές διαδρομές
(καθυστέρηση διάδοσης)

2^η Εργαστηριακή Άσκηση

Implementation – Timing Reports (2/2)

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Logic %	Net %	Requirement	Source Clock	Destination Clock	Exception	Site	
Unconstrained Paths (1)																	
(none) (8)																	
Path 1	∞	3	2	7	bcd[1]	seven_segment[0]	3.918	1.537	2.382	39.2	60.8	-∞	input port clock				
Path 2	∞	2	1	1	digit_selection_in	digit_selection_out	3.959	1.539	2.419	38.9	61.1	-∞	input port clock				
Path 3	∞	3	2	7	bcd[1]	seven_segment[1]	4.217	1.598	2.619	37.9	62.1	-∞	input port clock				
Path 4	∞	3	2	7	bcd[1]	seven_segment[4]	4.223	1.708	2.516	40.4	59.6	-∞	input port clock				
Path 5	∞	3	2	7	bcd[1]	seven_segment[3]	4.259	1.560	2.699	36.6	63.4	-∞	input port clock				
Path 6	∞	3	2	7	bcd[1]	seven_segment[5]	4.285	1.714	2.571	40.0	60.0	-∞	input port clock				
Path 7	∞	3	2	7	bcd[1]	seven_segment[0]	4.300	1.651	2.649	38.4	61.6	-∞	input port clock				
Path 8	∞	3	2	7	bcd[1]	seven_segment[2]	4.336	1.642	2.694	37.9	62.1	-∞	input port clock				

Hold Time:

Αναφέρεται στις γρήγορες διαδρομές
(καθυστέρηση μόλυνσης)

2^η Εργαστηριακή Άσκηση

Implementation – Path Analysis

The screenshot displays the Xilinx Vivado implementation environment. The main window shows the 'Path 9 - timing_1' analysis. The 'Data Path' table provides a detailed breakdown of the path's delay components:

Delay Type	Incr (ns)	Path (ns)	Location	Netlist Resource(s)
net (fo=0)	0.000	0.000	Site: F21	bcd[3]
IBUF (Prop. ibuf I O)	1.504	1.504	Site: F21	bcd_IBUF[3]_instI, bcd_IBUF[3]_instIO
net (fo=7, routed)	6.896	8.401	Site: S...X0Y42	bcd_IBUF[3]
LUT4 (Pro...I4 IO O)	0.150	8.551	Site: S...X0Y42	seven_segment_OBUF[2]_instI_1I0, seven_segment_OBUF[2]_instI_1IO
net (fo=1, routed)	2.083	10.634	Site: Y10	seven_segment_OBUF[2]
OBUF (Pr...buf I O)	3.799	14.432	Site: Y10	seven_segment_OBUF[2]_instI, seven_segment_OBUF[2]_instIO
net (fo=0)	0.000	14.432	Site: Y10	seven_segment[2]

The 'Timing Checks - Setup' table at the bottom provides a summary of timing constraints:

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Logic %	Net %	Requirement	Source Clock	Destination Clock	Exception
Unconstrained Paths (1)															
(none) (8)															
Path 9	∞	3	2	7	bcd[3]	seven_segment[2]	14.432	5.453	8.979	37.8	62.2	∞	input port clock		
Path 10	∞	3	2	7	bcd[3]	seven_segment[5]	14.246	5.540	8.706	38.9	61.1	∞	input port clock		
Path 11	∞	3	2	7	bcd[3]	seven_segment[3]	14.157	5.206	8.952	36.8	63.2	∞	input port clock		
Path 12	∞	3	2	7	bcd[0]	seven_segment[0]	14.110	5.449	8.661	38.6	61.4	∞	input port clock		

2^η Εργαστηριακή Άσκηση

Simulation

```
LIBRARY ieee; USE ieee.std_logic_1164.ALL; USE ieee.numeric_std.ALL;

entity bcd2sevenseg_tb IS
end bcd2sevenseg_tb;

architecture behavior OF bcd2sevenseg_tb IS
-- Component Declaration for the Unit Under Test (UUT)

    component bcd2sevenseg
    port (
        digit_selection_in  : in std_logic;
        bcd                 : in std_logic_vector(3 downto 0);
        seven_segment       : out std_logic_vector(6 downto 0);
        digit_selection_out  : out std_logic
    );
    end component;

    signal bcd          : std_logic_vector(3 downto 0) := (others => 'X');
    signal digit_selection_in  : std_logic;
    signal seven_segment      : std_logic_vector(6 downto 0);
    signal digit_selection_out : std_logic;

begin

    uut: bcd2sevenseg PORT MAP (digit_selection_in => digit_selection_in,
                                bcd => bcd,
                                seven_segment => seven_segment,
                                digit_selection_out => digit_selection_out );

    test_proc: process is
    begin

        bcd<="0001"; digit_selection_in<='1';wait for 20ns;
        bcd<="0100";wait for 20ns;
        bcd<="1001"; digit_selection_in<='0';wait for 20ns;
        bcd<="1011";wait for 20ns;

    end process test_proc;

end architecture behavior;
```

2^η Εργαστηριακή Άσκηση

Simulation - Behavioral

The screenshot displays a behavioral simulation window for a BCD-to-7-segment converter. The window is divided into three main sections:

- Scope Table:** Lists the design units and their types. The selected unit is `bcd2sev7seg` of type `VHDL E`.
- Objects Table:** Shows the current state of objects. The selected object is `bcd[3:0]` with a value of `9` and data type `Array`.
- Waveform Plot:** Shows the timing of signals over 150 ns. The signals are `bcd[3:0]`, `digit_selection_in`, `seven_segment[6:0]`, and `digit_selection_out`. The waveform shows the BCD input changing from 0001 to 1001, and the corresponding 7-segment outputs and digit selection signals.

Name	Value	Data Type
bcd[3:0]	9	Array
digit_selection_0		Logic
seven_segmen	6f	Array
digit_selection_0		Logic

Name	Value
bcd[3:0]	1001
digit_selection_in	0
seven_segment[6:0]	1101111
digit_selection_out	0

Waveform Plot (Time: 0.000 ns to 150.000 ns):

- `bcd[3:0]`: 0001, 0100, 1001, 1011, 0001, 0100, 1001, 1011, 0001
- `digit_selection_in`: 0, 0, 0, 0, 0, 0, 0, 0, 0
- `seven_segment[6:0]`: 0000110, 1100110, 1101111, 1000000, 0000110, 1100110, 1101111, 1000000, 0000110
- `digit_selection_out`: 0, 0, 0, 0, 0, 0, 0, 0, 0

2^η Εργαστηριακή Άσκηση

Simulation – Post Synthesis Timing Simulation

