NVIDIACUDA Toolkit Documentation

Αρχή φόρμας



Τέλος φόρμας

[CUDA Toolkit v7.0](http://docs.nvidia.com/cuda/index.html)

[Programming Guide](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html)

* ▽[1. Introduction](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#introduction)
  + [1.1. From Graphics Processing to General Purpose Parallel Computing](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#from-graphics-processing-to-general-purpose-parallel-computing)
  + [1.2. CUDA: A General-Purpose Parallel Computing Platform and Programming Model](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#cuda-general-purpose-parallel-computing-architecture)
  + [1.3. A Scalable Programming Model](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#scalable-programming-model)
  + [1.4. Document Structure](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#document-structure)
* ▽[2. Programming Model](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#programming-model)
  + [2.1. Kernels](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#kernels)
  + [2.2. Thread Hierarchy](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#thread-hierarchy)
  + [2.3. Memory Hierarchy](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#memory-hierarchy)
  + [2.4. Heterogeneous Programming](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#heterogeneous-programming)
  + [2.5. Compute Capability](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compute-capability)
* ▽[3. Programming Interface](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#programming-interface)
  + ▽[3.1. Compilation with NVCC](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compilation-with-nvcc)
    - ▽[3.1.1. Compilation Workflow](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compilation-workflow)
      * [3.1.1.1. Offline Compilation](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#offline-compilation)
      * [3.1.1.2. Just-in-Time Compilation](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#just-in-time-compilation)
    - [3.1.2. Binary Compatibility](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#binary-compatibility)
    - [3.1.3. PTX Compatibility](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#ptx-compatibility)
    - [3.1.4. Application Compatibility](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#application-compatibility)
    - [3.1.5. C/C++ Compatibility](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#c-cplusplus-compatibility)
    - [3.1.6. 64-Bit Compatibility](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#sixtyfour-bit-compatibility)
  + ▷[3.2. CUDA C Runtime](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#cuda-c-runtime)
  + [3.3. Versioning and Compatibility](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#versioning-and-compatibility)
  + [3.4. Compute Modes](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compute-modes)
  + [3.5. Mode Switches](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#mode-switches)
  + [3.6. Tesla Compute Cluster Mode for Windows](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#tesla-compute-cluster-mode-for-windows)
* ▷[4. Hardware Implementation](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#hardware-implementation)
* ▷[5. Performance Guidelines](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#performance-guidelines)
* [A. CUDA-Enabled GPUs](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#cuda-enabled-gpus)
* ▷[B. C Language Extensions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#c-language-extensions)
* ▷[C. CUDA Dynamic Parallelism](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#cuda-dynamic-parallelism)
* ▷[D. Mathematical Functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#mathematical-functions-appendix)
* ▷[E. C/C++ Language Support](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#c-cplusplus-language-support)
* ▷[F. Texture Fetching](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texture-fetching)
* ▷[G. Compute Capabilities](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compute-capabilities)
* ▷[H. Driver API](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#driver-api)
* [I. CUDA Environment Variables](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#env-vars)
* ▷[J. Unified Memory Programming](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#um-unified-memory-programming-hd)

Programming Guide ([PDF](http://docs.nvidia.com/cuda/pdf/CUDA_C_Programming_Guide.pdf)) - v7.0 ([older](https://developer.nvidia.com/cuda-toolkit-archive)) - Last updated March 5, 2015 - [Send Feedback](mailto:cudatools@nvidia.com?subject=CUDA%20Toolkit%20Documentation%20Feedback:%20Programming%20Guide) -

## [CUDA C Programming Guide](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "abstract)

## [Changes from Version 6.5](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "changes-from-previous-version)

* Removed all references to devices of compute capabilities 1.x as they are no longer supported.
* Mentioned in [Default Stream](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#default-stream) the new --default-stream compilation flag that changes the behavior of the default stream.
* Clarified the behavior of some atomic operations in [Floating-Point Standard](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#floating-point-standard).
* Updated [Table 6](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#standard-functions__single-precision-stdlib) for improved ULP errors for rhypotf, rcbrtf, log2f, log10f, erfinvf, erfcf, erfcxf, and normcdff.
* Updated [Table 14](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#env-vars__cuda-environment-variables) as CUDA\_VISIBLE\_DEVICES now accepts gpu-uuids to enumerate devices.
* Added the new CUDA\_AUTO\_BOOST environment variable to [Table 14](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#env-vars__cuda-environment-variables).

## [1. Introduction](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "introduction)

### [1.1. From Graphics Processing to General Purpose Parallel Computing](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#from-graphics-processing-to-general-purpose-parallel-computing)

Driven by the insatiable market demand for realtime, high-definition 3D graphics, the programmable Graphic Processor Unit or GPU has evolved into a highly parallel, multithreaded, manycore processor with tremendous computational horsepower and very high memory bandwidth, as illustrated by [Figure 1](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#from-graphics-processing-to-general-purpose-parallel-computing__floating-point-operations-per-second-for-cpu-and-gpu) and [Figure 2](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#from-graphics-processing-to-general-purpose-parallel-computing__memory-bandwidth-for-cpu-and-gpu).

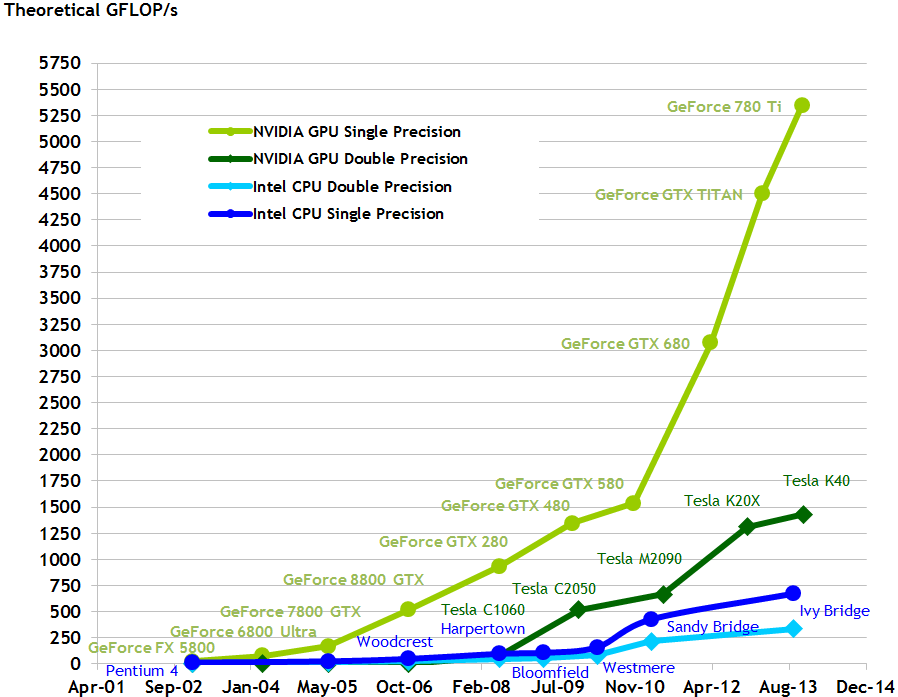
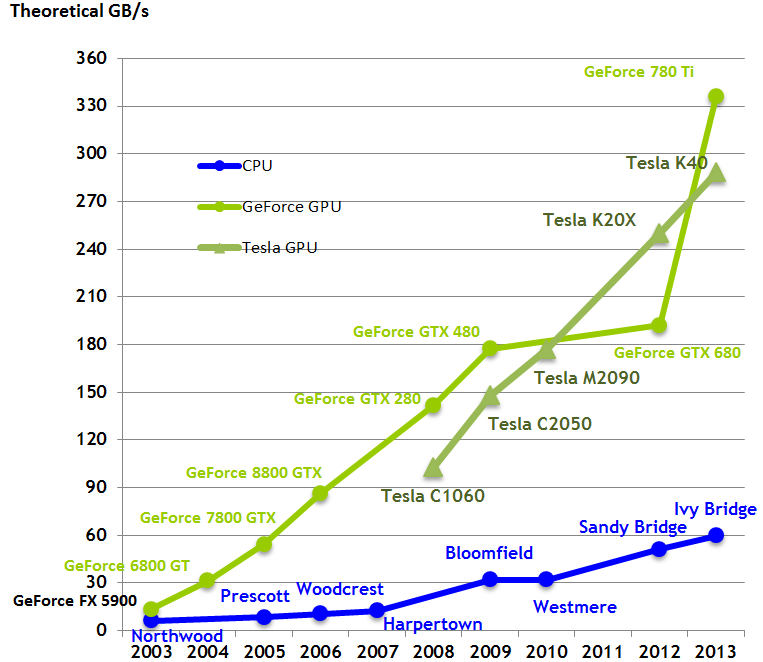
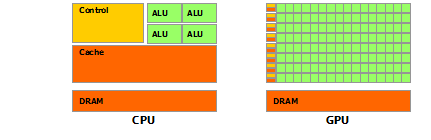
Figure 1. Floating-Point Operations per Second for the CPU and GPU  
  


Figure 2. Memory Bandwidth for the CPU and GPU  
  


The reason behind the discrepancy in floating-point capability between the CPU and the GPU is that the GPU is specialized for compute-intensive, highly parallel computation - exactly what graphics rendering is about - and therefore designed such that more transistors are devoted to data processing rather than data caching and flow control, as schematically illustrated by [Figure 3](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#from-graphics-processing-to-general-purpose-parallel-computing__gpu-devotes-more-transistors-to-data-processing).

Figure 3. The GPU Devotes More Transistors to Data Processing  
  


More specifically, the GPU is especially well-suited to address problems that can be expressed as data-parallel computations - the same program is executed on many data elements in parallel - with high arithmetic intensity - the ratio of arithmetic operations to memory operations. Because the same program is executed for each data element, there is a lower requirement for sophisticated flow control, and because it is executed on many data elements and has high arithmetic intensity, the memory access latency can be hidden with calculations instead of big data caches.

Data-parallel processing maps data elements to parallel processing threads. Many applications that process large data sets can use a data-parallel programming model to speed up the computations. In 3D rendering, large sets of pixels and vertices are mapped to parallel threads. Similarly, image and media processing applications such as post-processing of rendered images, video encoding and decoding, image scaling, stereo vision, and pattern recognition can map image blocks and pixels to parallel processing threads. In fact, many algorithms outside the field of image rendering and processing are accelerated by data-parallel processing, from general signal processing or physics simulation to computational finance or computational biology.

### [1.2. CUDA®: A General-Purpose Parallel Computing Platform and Programming Model](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#cuda-general-purpose-parallel-computing-architecture)

In November 2006, NVIDIA introduced CUDA®, a general purpose parallel computing platform and programming model that leverages the parallel compute engine in NVIDIA GPUs to solve many complex computational problems in a more efficient way than on a CPU.

CUDA comes with a software environment that allows developers to use C as a high-level programming language. As illustrated by [Figure 4](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#cuda-general-purpose-parallel-computing-architecture__cuda-is-designed-to-support-various-languages-and-application-programming-interfaces), other languages, application programming interfaces, or directives-based approaches are supported, such as FORTRAN, DirectCompute, OpenACC.

Figure 4. GPU Computing Applications. CUDA is designed to support various languages and application programming interfaces.



### [1.3. A Scalable Programming Model](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "scalable-programming-model)

The advent of multicore CPUs and manycore GPUs means that mainstream processor chips are now parallel systems. Furthermore, their parallelism continues to scale with Moore's law. The challenge is to develop application software that transparently scales its parallelism to leverage the increasing number of processor cores, much as 3D graphics applications transparently scale their parallelism to manycore GPUs with widely varying numbers of cores.

The CUDA parallel programming model is designed to overcome this challenge while maintaining a low learning curve for programmers familiar with standard programming languages such as C.

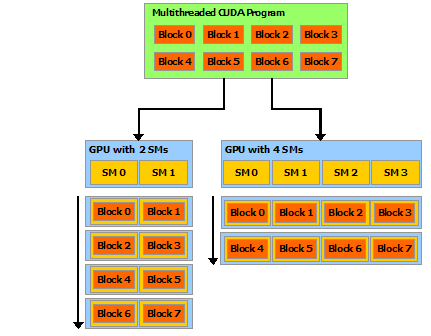
At its core are three key abstractions - a hierarchy of thread groups, shared memories, and barrier synchronization - that are simply exposed to the programmer as a minimal set of language extensions.

These abstractions provide fine-grained data parallelism and thread parallelism, nested within coarse-grained data parallelism and task parallelism. They guide the programmer to partition the problem into coarse sub-problems that can be solved independently in parallel by blocks of threads, and each sub-problem into finer pieces that can be solved cooperatively in parallel by all threads within the block.

This decomposition preserves language expressivity by allowing threads to cooperate when solving each sub-problem, and at the same time enables automatic scalability. Indeed, each block of threads can be scheduled on any of the available multiprocessors within a GPU, in any order, concurrently or sequentially, so that a compiled CUDA program can execute on any number of multiprocessors as illustrated by [Figure 5](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#scalable-programming-model__automatic-scalability), and only the runtime system needs to know the physical multiprocessor count.

This scalable programming model allows the GPU architecture to span a wide market range by simply scaling the number of multiprocessors and memory partitions: from the high-performance enthusiast GeForce GPUs and professional Quadro and Tesla computing products to a variety of inexpensive, mainstream GeForce GPUs (see [CUDA-Enabled GPUs](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#cuda-enabled-gpus) for a list of all CUDA-enabled GPUs).

Figure 5. Automatic Scalability



Note: A GPU is built around an array of Streaming Multiprocessors (SMs) (see [Hardware Implementation](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#hardware-implementation) for more details). A multithreaded program is partitioned into blocks of threads that execute independently from each other, so that a GPU with more multiprocessors will automatically execute the program in less time than a GPU with fewer multiprocessors.

### [1.4. Document Structure](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "document-structure)

This document is organized into the following chapters:

* Chapter [Introduction](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#introduction) is a general introduction to CUDA.
* Chapter [Programming Model](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#programming-model) outlines the CUDA programming model.
* Chapter [Programming Interface](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#programming-interface) describes the programming interface.
* Chapter [Hardware Implementation](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#hardware-implementation) describes the hardware implementation.
* Chapter [Performance Guidelines](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#performance-guidelines) gives some guidance on how to achieve maximum performance.
* Appendix [CUDA-Enabled GPUs](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#cuda-enabled-gpus) lists all CUDA-enabled devices.
* Appendix [C Language Extensions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#c-language-extensions) is a detailed description of all extensions to the C language.
* Appendix [Mathematical Functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#mathematical-functions-appendix) lists the mathematical functions supported in CUDA.
* Appendix [C/C++ Language Support](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#c-cplusplus-language-support) lists the C++ features supported in device code.
* Appendix [Texture Fetching](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texture-fetching) gives more details on texture fetching
* Appendix [Compute Capabilities](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compute-capabilities) gives the technical specifications of various devices, as well as more architectural details.
* Appendix [Driver API](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#driver-api) introduces the low-level driver API.
* Appendix [CUDA Environment Variables](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#env-vars) lists all the CUDA environment variables.

## [2. Programming Model](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "programming-model)

This chapter introduces the main concepts behind the CUDA programming model by outlining how they are exposed in C. An extensive description of CUDA C is given in [Programming Interface](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#programming-interface).

Full code for the vector addition example used in this chapter and the next can be found in the vectorAdd CUDA sample.

### [2.1. Kernels](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "kernels)

CUDA C extends C by allowing the programmer to define C functions, called kernels, that, when called, are executed N times in parallel by N different CUDA threads, as opposed to only once like regular C functions.

A kernel is defined using the \_\_global\_\_ declaration specifier and the number of CUDA threads that execute that kernel for a given kernel call is specified using a new <<<...>>>execution configuration syntax (see [C Language Extensions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#c-language-extensions)). Each thread that executes the kernel is given a unique thread ID that is accessible within the kernel through the built-in threadIdx variable.

As an illustration, the following sample code adds two vectors A and B of size N and stores the result into vector C:

// Kernel definition

\_\_global\_\_ void VecAdd(float\* A, float\* B, float\* C)

{

int i = threadIdx.x;

C[i] = A[i] + B[i];

}

int main()

{

...

// Kernel invocation with N threads

VecAdd<<<1, N>>>(A, B, C);

...

}

Here, each of the N threads that execute VecAdd() performs one pair-wise addition.

### [2.2. Thread Hierarchy](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "thread-hierarchy)

For convenience, threadIdx is a 3-component vector, so that threads can be identified using a one-dimensional, two-dimensional, or three-dimensional thread index, forming a one-dimensional, two-dimensional, or three-dimensional thread block. This provides a natural way to invoke computation across the elements in a domain such as a vector, matrix, or volume.

The index of a thread and its thread ID relate to each other in a straightforward way: For a one-dimensional block, they are the same; for a two-dimensional block of size (Dx, Dy),the thread ID of a thread of index (x, y) is (x + y Dx); for a three-dimensional block of size (Dx, Dy, Dz), the thread ID of a thread of index (x, y, z) is (x + y Dx + z Dx Dy).

As an example, the following code adds two matrices A and B of size NxN and stores the result into matrix C:

// Kernel definition

\_\_global\_\_ void MatAdd(float A[N][N], float B[N][N],

float C[N][N])

{

int i = threadIdx.x;

int j = threadIdx.y;

C[i][j] = A[i][j] + B[i][j];

}

int main()

{

...

// Kernel invocation with one block of N \* N \* 1 threads

int numBlocks = 1;

dim3 threadsPerBlock(N, N);

MatAdd<<<numBlocks, threadsPerBlock>>>(A, B, C);

...

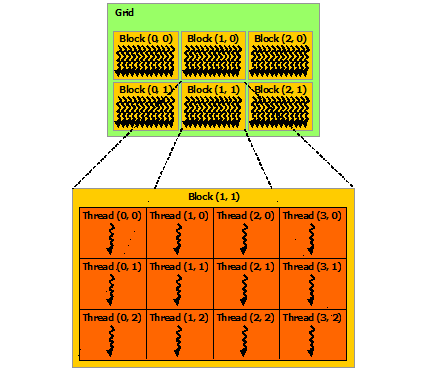
}

There is a limit to the number of threads per block, since all threads of a block are expected to reside on the same processor core and must share the limited memory resources of that core. On current GPUs, a thread block may contain up to 1024 threads.

However, a kernel can be executed by multiple equally-shaped thread blocks, so that the total number of threads is equal to the number of threads per block times the number of blocks.

Blocks are organized into a one-dimensional, two-dimensional, or three-dimensional grid of thread blocks as illustrated by [Figure 6](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#thread-hierarchy__grid-of-thread-blocks). The number of thread blocks in a grid is usually dictated by the size of the data being processed or the number of processors in the system, which it can greatly exceed.

Figure 6. Grid of Thread Blocks



The number of threads per block and the number of blocks per grid specified in the <<<...>>> syntax can be of type int or dim3. Two-dimensional blocks or grids can be specified as in the example above.

Each block within the grid can be identified by a one-dimensional, two-dimensional, or three-dimensional index accessible within the kernel through the built-in blockIdx variable. The dimension of the thread block is accessible within the kernel through the built-in blockDim variable.

Extending the previous MatAdd() example to handle multiple blocks, the code becomes as follows.

// Kernel definition

\_\_global\_\_ void MatAdd(float A[N][N], float B[N][N],

float C[N][N])

{

int i = blockIdx.x \* blockDim.x + threadIdx.x;

int j = blockIdx.y \* blockDim.y + threadIdx.y;

if (i < N && j < N)

C[i][j] = A[i][j] + B[i][j];

}

int main()

{

...

// Kernel invocation

dim3 threadsPerBlock(16, 16);

dim3 numBlocks(N / threadsPerBlock.x, N / threadsPerBlock.y);

MatAdd<<<numBlocks, threadsPerBlock>>>(A, B, C);

...

}

A thread block size of 16x16 (256 threads), although arbitrary in this case, is a common choice. The grid is created with enough blocks to have one thread per matrix element as before. For simplicity, this example assumes that the number of threads per grid in each dimension is evenly divisible by the number of threads per block in that dimension, although that need not be the case.

Thread blocks are required to execute independently: It must be possible to execute them in any order, in parallel or in series. This independence requirement allows thread blocks to be scheduled in any order across any number of cores as illustrated by Figure 1 4, enabling programmers to write code that scales with the number of cores.

Threads within a block can cooperate by sharing data through some shared memory and by synchronizing their execution to coordinate memory accesses. More precisely, one can specify synchronization points in the kernel by calling the \_\_syncthreads() intrinsic function; \_\_syncthreads() acts as a barrier at which all threads in the block must wait before any is allowed to proceed. [Shared Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#shared-memory) gives an example of using shared memory.

For efficient cooperation, the shared memory is expected to be a low-latency memory near each processor core (much like an L1 cache) and \_\_syncthreads() is expected to be lightweight.

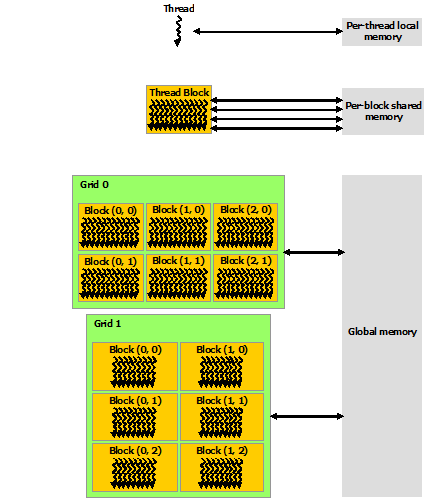
### [2.3. Memory Hierarchy](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "memory-hierarchy)

CUDA threads may access data from multiple memory spaces during their execution as illustrated by [Figure 7](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#memory-hierarchy__memory-hierarchy-figure). Each thread has private local memory. Each thread block has shared memory visible to all threads of the block and with the same lifetime as the block. All threads have access to the same global memory.

There are also two additional read-only memory spaces accessible by all threads: the constant and texture memory spaces. The global, constant, and texture memory spaces are optimized for different memory usages (see [Device Memory Accesses](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#device-memory-accesses)). Texture memory also offers different addressing modes, as well as data filtering, for some specific data formats (see [Texture and Surface Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texture-and-surface-memory)).

The global, constant, and texture memory spaces are persistent across kernel launches by the same application.

Figure 7. Memory Hierarchy

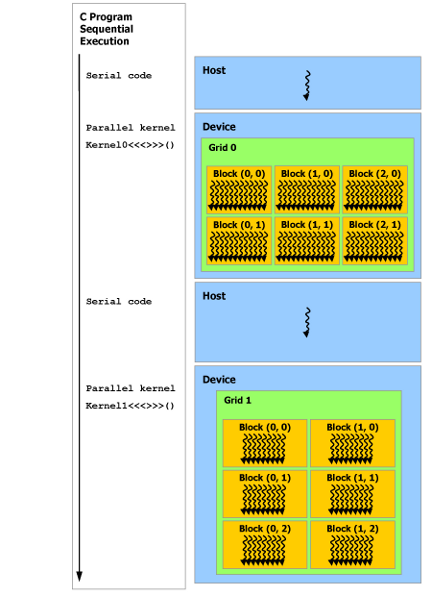


### [2.4. Heterogeneous Programming](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "heterogeneous-programming)

As illustrated by [Figure 8](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#heterogeneous-programming__heterogeneous-programming), the CUDA programming model assumes that the CUDA threads execute on a physically separate device that operates as a coprocessor to the host running the C program. This is the case, for example, when the kernels execute on a GPU and the rest of the C program executes on a CPU.

The CUDA programming model also assumes that both the host and the device maintain their own separate memory spaces in DRAM, referred to as host memory and device memory, respectively. Therefore, a program manages the global, constant, and texture memory spaces visible to kernels through calls to the CUDA runtime (described in [Programming Interface](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#programming-interface)). This includes device memory allocation and deallocation as well as data transfer between host and device memory.

Figure 8. Heterogeneous Programming



Note: Serial code executes on the host while parallel code executes on the device.

### [2.5. Compute Capability](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "compute-capability)

The compute capability of a device is represented by a version number, also sometimes called its "SM version". This version number identifies the features supported by the GPU hardware and is used by applications at runtime to determine which hardware features and/or instructions are available on the present GPU.

The compute capability version comprises a major and a minor version number (x.y):

Devices with the same major revision number are of the same core architecture. The major revision number is 5 for devices based on the Maxwell architecture, 3 for devices based on the Kepler architecture, 2 for devices based on the Fermi architecture, and 1 for devices based on the Tesla architecture.

The minor revision number corresponds to an incremental improvement to the core architecture, possibly including new features.

[CUDA-Enabled GPUs](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#cuda-enabled-gpus) lists of all CUDA-enabled devices along with their compute capability. [Compute Capabilities](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compute-capabilities) gives the technical specifications of each compute capability.

Note: The compute capability version of a particular GPU should not be confused with the CUDA version (e.g., CUDA 5.5, CUDA 6, CUDA 6.5), which is the version of the CUDA software platform. The CUDA platform is used by application developers to create applications that run on many generations of GPU architectures, including future GPU architectures yet to be invented. While new versions of the CUDA platform often add native support for a new GPU architecture by supporting the compute capability version of that architecture, new versions of the CUDA platform typically also include software features that are independent of hardware generation.

The Tesla architecture is no longer supported starting with CUDA 7.0.

## [3. Programming Interface](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "programming-interface)

CUDA C provides a simple path for users familiar with the C programming language to easily write programs for execution by the device.

It consists of a minimal set of extensions to the C language and a runtime library.

The core language extensions have been introduced in [Programming Model](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#programming-model). They allow programmers to define a kernel as a C function and use some new syntax to specify the grid and block dimension each time the function is called. A complete description of all extensions can be found in [C Language Extensions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#c-language-extensions). Any source file that contains some of these extensions must be compiled with nvcc as outlined in [Compilation with NVCC](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compilation-with-nvcc).

The runtime is introduced in [Compilation Workflow](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compilation-workflow). It provides C functions that execute on the host to allocate and deallocate device memory, transfer data between host memory and device memory, manage systems with multiple devices, etc. A complete description of the runtime can be found in the CUDA reference manual.

The runtime is built on top of a lower-level C API, the CUDA driver API, which is also accessible by the application. The driver API provides an additional level of control by exposing lower-level concepts such as CUDA contexts - the analogue of host processes for the device - and CUDA modules - the analogue of dynamically loaded libraries for the device. Most applications do not use the driver API as they do not need this additional level of control and when using the runtime, context and module management are implicit, resulting in more concise code. The driver API is introduced in [Driver API](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#driver-api) and fully described in the reference manual.

### [3.1. Compilation with NVCC](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "compilation-with-nvcc)

Kernels can be written using the CUDA instruction set architecture, called PTX, which is described in the PTX reference manual. It is however usually more effective to use a high-level programming language such as C. In both cases, kernels must be compiled into binary code by nvcc to execute on the device.

nvcc is a compiler driver that simplifies the process of compiling C or PTX code: It provides simple and familiar command line options and executes them by invoking the collection of tools that implement the different compilation stages. This section gives an overview of nvcc workflow and command options. A complete description can be found in the nvcc user manual.

### [3.1.1. Compilation Workflow](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "compilation-workflow)

### [3.1.1.1. Offline Compilation](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "offline-compilation)

Source files compiled with nvcc can include a mix of host code (i.e., code that executes on the host) and device code (i.e., code that executes on the device). nvcc's basic workflow consists in separating device code from host code and then:

* compiling the device code into an assembly form (PTX code) and/or binary form (cubin object),
* and modifying the host code by replacing the <<<...>>> syntax introduced in [Kernels](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#kernels) (and described in more details in [Execution Configuration](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#execution-configuration)) by the necessary CUDA C runtime function calls to load and launch each compiled kernel from the PTX code and/or cubin object.

The modified host code is output either as C code that is left to be compiled using another tool or as object code directly by letting nvcc invoke the host compiler during the last compilation stage.

Applications can then:

* Either link to the compiled host code (this is the most common case),
* Or ignore the modified host code (if any) and use the CUDA driver API (see [Driver API](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#driver-api)) to load and execute the PTX code or cubin object.

### [3.1.1.2. Just-in-Time Compilation](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "just-in-time-compilation)

Any PTX code loaded by an application at runtime is compiled further to binary code by the device driver. This is called just-in-time compilation. Just-in-time compilation increases application load time, but allows the application to benefit from any new compiler improvements coming with each new device driver. It is also the only way for applications to run on devices that did not exist at the time the application was compiled, as detailed in [Application Compatibility](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#application-compatibility).

When the device driver just-in-time compiles some PTX code for some application, it automatically caches a copy of the generated binary code in order to avoid repeating the compilation in subsequent invocations of the application. The cache - referred to as compute cache - is automatically invalidated when the device driver is upgraded, so that applications can benefit from the improvements in the new just-in-time compiler built into the device driver.

Environment variables are available to control just-in-time compilation as described in [CUDA Environment Variables](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#env-vars)

### [3.1.2. Binary Compatibility](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "binary-compatibility)

Binary code is architecture-specific. A cubin object is generated using the compiler option -code that specifies the targeted architecture: For example, compiling with -code=sm\_35 produces binary code for devices of [compute capability](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compute-capability) 3.5. Binary compatibility is guaranteed from one minor revision to the next one, but not from one minor revision to the previous one or across major revisions. In other words, a cubin object generated for compute capability X.y will only execute on devices of compute capability X.z where z≥y.

### [3.1.3. PTX Compatibility](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "ptx-compatibility)

Some PTX instructions are only supported on devices of higher compute capabilities. For example, warp shuffle instructions are only supported on devices of compute capability 3.0 and above. The -arch compiler option specifies the compute capability that is assumed when compiling C to PTX code. So, code that contains warp shuffle, for example, must be compiled with -arch=sm\_30 (or higher).

PTX code produced for some specific compute capability can always be compiled to binary code of greater or equal compute capability.

### [3.1.4. Application Compatibility](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "application-compatibility)

To execute code on devices of specific compute capability, an application must load binary or PTX code that is compatible with this compute capability as described in [Binary Compatibility](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#binary-compatibility) and [PTX Compatibility](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#ptx-compatibility). In particular, to be able to execute code on future architectures with higher compute capability (for which no binary code can be generated yet), an application must load PTX code that will be just-in-time compiled for these devices (see [Just-in-Time Compilation](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#just-in-time-compilation)).

Which PTX and binary code gets embedded in a CUDA C application is controlled by the -arch and -code compiler options or the -gencode compiler option as detailed in the nvcc user manual. For example,

nvcc x.cu

-gencode arch=compute\_20,code=sm\_20

-gencode arch=compute\_30,code=sm\_30

-gencode arch=compute\_35,code=\'compute\_35,sm\_35\'

embeds binary code compatible with compute capability 2.0 and 3.0 (first and second -gencode options) and PTX and binary code compatible with compute capability 3.5 (third -gencode option).

Host code is generated to automatically select at runtime the most appropriate code to load and execute, which, in the above example, will be:

* 2.0 binary code for devices with compute capability 2.0 and 2.1,
* 3.0 binary code for devices with compute capability 3.0,
* 3.5 binary code for devices with compute capability 3.5 and higher 3.x,
* binary code obtained by compiling 3.5 PTX code for devices with compute capabilities 3.5 and higher.

x.cu can have an optimized code path that uses warp shuffle operations, for example, which are only supported in devices of compute capability 3.0 and higher. The \_\_CUDA\_ARCH\_\_ macro can be used to differentiate various code paths based on compute capability. It is only defined for device code. When compiling with -arch=compute\_35 for example, \_\_CUDA\_ARCH\_\_ is equal to 350.

Applications using the driver API must compile code to separate files and explicitly load and execute the most appropriate file at runtime.

The nvcc user manual lists various shorthand for the -arch, -code, and -gencode compiler options. For example, -arch=sm\_35 is a shorthand for -arch=compute\_35-code=compute\_35,sm\_35 (which is the same as -gencodearch=compute\_35,code=\'compute\_35,sm\_35\').

### [3.1.5. C/C++ Compatibility](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "c-cplusplus-compatibility)

The front end of the compiler processes CUDA source files according to C++ syntax rules. Full C++ is supported for the host code. However, only a subset of C++ is fully supported for the device code as described in [C/C++ Language Support](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#c-cplusplus-language-support).

### [3.1.6. 64-Bit Compatibility](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "sixtyfour-bit-compatibility)

The 64-bit version of nvcc compiles device code in 64-bit mode (i.e., pointers are 64-bit). Device code compiled in 64-bit mode is only supported with host code compiled in 64-bit mode.

Similarly, the 32-bit version of nvcc compiles device code in 32-bit mode and device code compiled in 32-bit mode is only supported with host code compiled in 32-bit mode.

The 32-bit version of nvcc can compile device code in 64-bit mode also using the -m64 compiler option.

The 64-bit version of nvcc can compile device code in 32-bit mode also using the -m32 compiler option.

### [3.2. CUDA C Runtime](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "cuda-c-runtime)

The runtime is implemented in the cudart library, which is linked to the application, either statically via cudart.lib or libcudart.a, or dynamically via cudart.dll or libcudart.so. Applications that require cudart.dll and/or cudart.so for dynamic linking typically include them as part of the application installation package.

All its entry points are prefixed with cuda.

As mentioned in [Heterogeneous Programming](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#heterogeneous-programming), the CUDA programming model assumes a system composed of a host and a device, each with their own separate memory. [Device Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#device-memory) gives an overview of the runtime functions used to manage device memory.

[Shared Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#shared-memory) illustrates the use of shared memory, introduced in [Thread Hierarchy](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#thread-hierarchy), to maximize performance.

[Page-Locked Host Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#page-locked-host-memory) introduces page-locked host memory that is required to overlap kernel execution with data transfers between host and device memory.

[Asynchronous Concurrent Execution](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#asynchronous-concurrent-execution) describes the concepts and API used to enable asynchronous concurrent execution at various levels in the system.

[Multi-Device System](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#multi-device-system) shows how the programming model extends to a system with multiple devices attached to the same host.

[Error Checking](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#error-checking) describes how to properly check the errors generated by the runtime.

[Call Stack](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#call-stack) mentions the runtime functions used to manage the CUDA C call stack.

[Texture and Surface Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texture-and-surface-memory) presents the texture and surface memory spaces that provide another way to access device memory; they also expose a subset of the GPU texturing hardware.

[Graphics Interoperability](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#graphics-interoperability) introduces the various functions the runtime provides to interoperate with the two main graphics APIs, OpenGL and Direct3D.

### [3.2.1. Initialization](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "initialization)

There is no explicit initialization function for the runtime; it initializes the first time a runtime function is called (more specifically any function other than functions from the device and version management sections of the reference manual). One needs to keep this in mind when timing runtime function calls and when interpreting the error code from the first call into the runtime.

During initialization, the runtime creates a CUDA context for each device in the system (see [Context](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#context) for more details on CUDA contexts). This context is the primary context for this device and it is shared among all the host threads of the application. As part of this context creation, the device code is just-in-time compiled if necessary (see [Just-in-Time Compilation](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#just-in-time-compilation)) and loaded into device memory. This all happens under the hood and the runtime does not expose the primary context to the application.

When a host thread calls cudaDeviceReset(), this destroys the primary context of the device the host thread currently operates on (i.e., the current device as defined in [Device Selection](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#device-selection)). The next runtime function call made by any host thread that has this device as current will create a new primary context for this device.

### [3.2.2. Device Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "device-memory)

As mentioned in [Heterogeneous Programming](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#heterogeneous-programming), the CUDA programming model assumes a system composed of a host and a device, each with their own separate memory. Kernels operate out of device memory, so the runtime provides functions to allocate, deallocate, and copy device memory, as well as transfer data between host memory and device memory.

Device memory can be allocated either as linear memory or as CUDA arrays.

CUDA arrays are opaque memory layouts optimized for texture fetching. They are described in [Texture and Surface Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texture-and-surface-memory).

Linear memory exists on the device in a 40-bit address space, so separately allocated entities can reference one another via pointers, for example, in a binary tree.

Linear memory is typically allocated using cudaMalloc() and freed using cudaFree() and data transfer between host memory and device memory are typically done using cudaMemcpy(). In the vector addition code sample of [Kernels](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#kernels), the vectors need to be copied from host memory to device memory:

// Device code

\_\_global\_\_ void VecAdd(float\* A, float\* B, float\* C, int N)

{

int i = blockDim.x \* blockIdx.x + threadIdx.x;

if (i < N)

C[i] = A[i] + B[i];

}

// Host code

int main()

{

int N = ...;

size\_t size = N \* sizeof(float);

// Allocate input vectors h\_A and h\_B in host memory

float\* h\_A = (float\*)malloc(size);

float\* h\_B = (float\*)malloc(size);

// Initialize input vectors

...

// Allocate vectors in device memory

float\* d\_A;

cudaMalloc(&d\_A, size);

float\* d\_B;

cudaMalloc(&d\_B, size);

float\* d\_C;

cudaMalloc(&d\_C, size);

// Copy vectors from host memory to device memory

cudaMemcpy(d\_A, h\_A, size, cudaMemcpyHostToDevice);

cudaMemcpy(d\_B, h\_B, size, cudaMemcpyHostToDevice);

// Invoke kernel

int threadsPerBlock = 256;

int blocksPerGrid =

(N + threadsPerBlock - 1) / threadsPerBlock;

VecAdd<<<blocksPerGrid, threadsPerBlock>>>(d\_A, d\_B, d\_C, N);

// Copy result from device memory to host memory

// h\_C contains the result in host memory

cudaMemcpy(h\_C, d\_C, size, cudaMemcpyDeviceToHost);

// Free device memory

cudaFree(d\_A);

cudaFree(d\_B);

cudaFree(d\_C);

// Free host memory

...

}

Linear memory can also be allocated through cudaMallocPitch() and cudaMalloc3D(). These functions are recommended for allocations of 2D or 3D arrays as it makes sure that the allocation is appropriately padded to meet the alignment requirements described in [Device Memory Accesses](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#device-memory-accesses), therefore ensuring best performance when accessing the row addresses or performing copies between 2D arrays and other regions of device memory (using the cudaMemcpy2D() and cudaMemcpy3D() functions). The returned pitch (or stride) must be used to access array elements. The following code sample allocates a width x height 2D array of floating-point values and shows how to loop over the array elements in device code:

// Host code

int width = 64, height = 64;

float\* devPtr;

size\_t pitch;

cudaMallocPitch(&devPtr, &pitch,

width \* sizeof(float), height);

MyKernel<<<100, 512>>>(devPtr, pitch, width, height);

// Device code

\_\_global\_\_ void MyKernel(float\* devPtr,

size\_t pitch, int width, int height)

{

for (int r = 0; r < height; ++r) {

float\* row = (float\*)((char\*)devPtr + r \* pitch);

for (int c = 0; c < width; ++c) {

float element = row[c];

}

}

}

The following code sample allocates a width x height x depth 3D array of floating-point values and shows how to loop over the array elements in device code:

// Host code

int width = 64, height = 64, depth = 64;

cudaExtent extent = make\_cudaExtent(width \* sizeof(float),

height, depth);

cudaPitchedPtr devPitchedPtr;

cudaMalloc3D(&devPitchedPtr, extent);

MyKernel<<<100, 512>>>(devPitchedPtr, width, height, depth);

// Device code

\_\_global\_\_ void MyKernel(cudaPitchedPtr devPitchedPtr,

int width, int height, int depth)

{

char\* devPtr = devPitchedPtr.ptr;

size\_t pitch = devPitchedPtr.pitch;

size\_t slicePitch = pitch \* height;

for (int z = 0; z < depth; ++z) {

char\* slice = devPtr + z \* slicePitch;

for (int y = 0; y < height; ++y) {

float\* row = (float\*)(slice + y \* pitch);

for (int x = 0; x < width; ++x) {

float element = row[x];

}

}

}

}

The reference manual lists all the various functions used to copy memory between linear memory allocated with cudaMalloc(), linear memory allocated with cudaMallocPitch() or cudaMalloc3D(), CUDA arrays, and memory allocated for variables declared in global or constant memory space.

The following code sample illustrates various ways of accessing global variables via the runtime API:

\_\_constant\_\_ float constData[256];

float data[256];

cudaMemcpyToSymbol(constData, data, sizeof(data));

cudaMemcpyFromSymbol(data, constData, sizeof(data));

\_\_device\_\_ float devData;

float value = 3.14f;

cudaMemcpyToSymbol(devData, &value, sizeof(float));

\_\_device\_\_ float\* devPointer;

float\* ptr;

cudaMalloc(&ptr, 256 \* sizeof(float));

cudaMemcpyToSymbol(devPointer, &ptr, sizeof(ptr));

cudaGetSymbolAddress() is used to retrieve the address pointing to the memory allocated for a variable declared in global memory space. The size of the allocated memory is obtained through cudaGetSymbolSize().

### [3.2.3. Shared Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "shared-memory)

As detailed in [Variable Type Qualifiers](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#variable-type-qualifiers) shared memory is allocated using the \_\_shared\_\_ qualifier.

Shared memory is expected to be much faster than global memory as mentioned in [Thread Hierarchy](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#thread-hierarchy) and detailed in [Shared Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#shared-memory). Any opportunity to replace global memory accesses by shared memory accesses should therefore be exploited as illustrated by the following matrix multiplication example.

The following code sample is a straightforward implementation of matrix multiplication that does not take advantage of shared memory. Each thread reads one row of A and one column of B and computes the corresponding element of C as illustrated in [Figure 9](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#shared-memory__matrix-multiplication-no-shared-memory). A is therefore read B.width times from global memory and B is read A.height times.

// Matrices are stored in row-major order:

// M(row, col) = \*(M.elements + row \* M.width + col)

typedef struct {

int width;

int height;

float\* elements;

} Matrix;

// Thread block size

#define BLOCK\_SIZE 16

// Forward declaration of the matrix multiplication kernel

\_\_global\_\_ void MatMulKernel(const Matrix, const Matrix, Matrix);

// Matrix multiplication - Host code

// Matrix dimensions are assumed to be multiples of BLOCK\_SIZE

void MatMul(const Matrix A, const Matrix B, Matrix C)

{

// Load A and B to device memory

Matrix d\_A;

d\_A.width = A.width; d\_A.height = A.height;

size\_t size = A.width \* A.height \* sizeof(float);

cudaMalloc(&d\_A.elements, size);

cudaMemcpy(d\_A.elements, A.elements, size,

cudaMemcpyHostToDevice);

Matrix d\_B;

d\_B.width = B.width; d\_B.height = B.height;

size = B.width \* B.height \* sizeof(float);

cudaMalloc(&d\_B.elements, size);

cudaMemcpy(d\_B.elements, B.elements, size,

cudaMemcpyHostToDevice);

// Allocate C in device memory

Matrix d\_C;

d\_C.width = C.width; d\_C.height = C.height;

size = C.width \* C.height \* sizeof(float);

cudaMalloc(&d\_C.elements, size);

// Invoke kernel

dim3 dimBlock(BLOCK\_SIZE, BLOCK\_SIZE);

dim3 dimGrid(B.width / dimBlock.x, A.height / dimBlock.y);

MatMulKernel<<<dimGrid, dimBlock>>>(d\_A, d\_B, d\_C);

// Read C from device memory

cudaMemcpy(C.elements, Cd.elements, size,

cudaMemcpyDeviceToHost);

// Free device memory

cudaFree(d\_A.elements);

cudaFree(d\_B.elements);

cudaFree(d\_C.elements);

}

// Matrix multiplication kernel called by MatMul()

\_\_global\_\_ void MatMulKernel(Matrix A, Matrix B, Matrix C)

{

// Each thread computes one element of C

// by accumulating results into Cvalue

float Cvalue = 0;

int row = blockIdx.y \* blockDim.y + threadIdx.y;

int col = blockIdx.x \* blockDim.x + threadIdx.x;

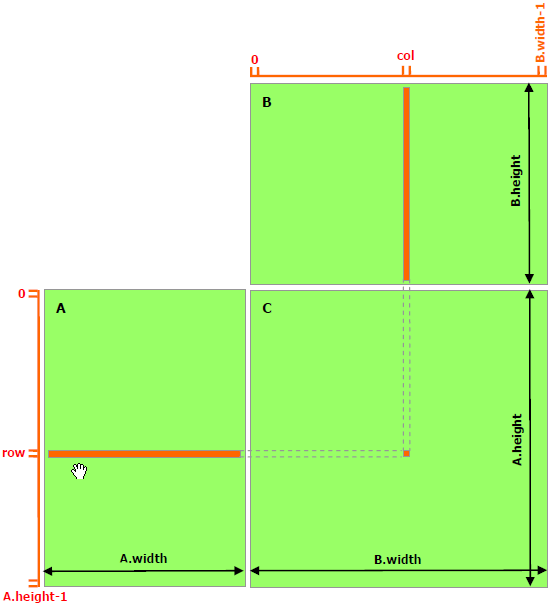
for (int e = 0; e < A.width; ++e)

Cvalue += A.elements[row \* A.width + e]

\* B.elements[e \* B.width + col];

C.elements[row \* C.width + col] = Cvalue;

}

Figure 9. Matrix Multiplication without Shared Memory  
  


The following code sample is an implementation of matrix multiplication that does take advantage of shared memory. In this implementation, each thread block is responsible for computing one square sub-matrix Csub of C and each thread within the block is responsible for computing one element of Csub. As illustrated in [Figure 10](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#shared-memory__matrix-multiplication-shared-memory), Csub is equal to the product of two rectangular matrices: the sub-matrix of A of dimension (A.width, block\_size) that has the same row indices as Csub, and the sub-matrix of B of dimension (block\_size, A.width )that has the same column indices as Csub. In order to fit into the device's resources, these two rectangular matrices are divided into as many square matrices of dimension block\_size as necessary and Csub is computed as the sum of the products of these square matrices. Each of these products is performed by first loading the two corresponding square matrices from global memory to shared memory with one thread loading one element of each matrix, and then by having each thread compute one element of the product. Each thread accumulates the result of each of these products into a register and once done writes the result to global memory.

By blocking the computation this way, we take advantage of fast shared memory and save a lot of global memory bandwidth since A is only read (B.width / block\_size) times from global memory and B is read (A.height / block\_size) times.

The Matrix type from the previous code sample is augmented with a stride field, so that sub-matrices can be efficiently represented with the same type. [\_\_device\_\_](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#device-function-qualifier) functions are used to get and set elements and build any sub-matrix from a matrix.

// Matrices are stored in row-major order:

// M(row, col) = \*(M.elements + row \* M.stride + col)

typedef struct {

int width;

int height;

int stride;

float\* elements;

} Matrix;

// Get a matrix element

\_\_device\_\_ float GetElement(const Matrix A, int row, int col)

{

return A.elements[row \* A.stride + col];

}

// Set a matrix element

\_\_device\_\_ void SetElement(Matrix A, int row, int col,

float value)

{

A.elements[row \* A.stride + col] = value;

}

// Get the BLOCK\_SIZExBLOCK\_SIZE sub-matrix Asub of A that is

// located col sub-matrices to the right and row sub-matrices down

// from the upper-left corner of A

\_\_device\_\_ Matrix GetSubMatrix(Matrix A, int row, int col)

{

Matrix Asub;

Asub.width = BLOCK\_SIZE;

Asub.height = BLOCK\_SIZE;

Asub.stride = A.stride;

Asub.elements = &A.elements[A.stride \* BLOCK\_SIZE \* row

+ BLOCK\_SIZE \* col];

return Asub;

}

// Thread block size

#define BLOCK\_SIZE 16

// Forward declaration of the matrix multiplication kernel

\_\_global\_\_ void MatMulKernel(const Matrix, const Matrix, Matrix);

// Matrix multiplication - Host code

// Matrix dimensions are assumed to be multiples of BLOCK\_SIZE

void MatMul(const Matrix A, const Matrix B, Matrix C)

{

// Load A and B to device memory

Matrix d\_A;

d\_A.width = d\_A.stride = A.width; d\_A.height = A.height;

size\_t size = A.width \* A.height \* sizeof(float);

cudaMalloc(&d\_A.elements, size);

cudaMemcpy(d\_A.elements, A.elements, size,

cudaMemcpyHostToDevice);

Matrix d\_B;

d\_B.width = d\_B.stride = B.width; d\_B.height = B.height;

size = B.width \* B.height \* sizeof(float);

cudaMalloc(&d\_B.elements, size);

cudaMemcpy(d\_B.elements, B.elements, size,

cudaMemcpyHostToDevice);

// Allocate C in device memory

Matrix d\_C;

d\_C.width = d\_C.stride = C.width; d\_C.height = C.height;

size = C.width \* C.height \* sizeof(float);

cudaMalloc(&d\_C.elements, size);

// Invoke kernel

dim3 dimBlock(BLOCK\_SIZE, BLOCK\_SIZE);

dim3 dimGrid(B.width / dimBlock.x, A.height / dimBlock.y);

MatMulKernel<<<dimGrid, dimBlock>>>(d\_A, d\_B, d\_C);

// Read C from device memory

cudaMemcpy(C.elements, d\_C.elements, size,

cudaMemcpyDeviceToHost);

// Free device memory

cudaFree(d\_A.elements);

cudaFree(d\_B.elements);

cudaFree(d\_C.elements);

}

// Matrix multiplication kernel called by MatMul()

\_\_global\_\_ void MatMulKernel(Matrix A, Matrix B, Matrix C)

{

// Block row and column

int blockRow = blockIdx.y;

int blockCol = blockIdx.x;

// Each thread block computes one sub-matrix Csub of C

Matrix Csub = GetSubMatrix(C, blockRow, blockCol);

// Each thread computes one element of Csub

// by accumulating results into Cvalue

float Cvalue = 0;

// Thread row and column within Csub

int row = threadIdx.y;

int col = threadIdx.x;

// Loop over all the sub-matrices of A and B that are

// required to compute Csub

// Multiply each pair of sub-matrices together

// and accumulate the results

for (int m = 0; m < (A.width / BLOCK\_SIZE); ++m) {

// Get sub-matrix Asub of A

Matrix Asub = GetSubMatrix(A, blockRow, m);

// Get sub-matrix Bsub of B

Matrix Bsub = GetSubMatrix(B, m, blockCol);

// Shared memory used to store Asub and Bsub respectively

\_\_shared\_\_ float As[BLOCK\_SIZE][BLOCK\_SIZE];

\_\_shared\_\_ float Bs[BLOCK\_SIZE][BLOCK\_SIZE];

// Load Asub and Bsub from device memory to shared memory

// Each thread loads one element of each sub-matrix

As[row][col] = GetElement(Asub, row, col);

Bs[row][col] = GetElement(Bsub, row, col);

// Synchronize to make sure the sub-matrices are loaded

// before starting the computation

\_\_syncthreads();

// Multiply Asub and Bsub together

for (int e = 0; e < BLOCK\_SIZE; ++e)

Cvalue += As[row][e] \* Bs[e][col];

// Synchronize to make sure that the preceding

// computation is done before loading two new

// sub-matrices of A and B in the next iteration

\_\_syncthreads();

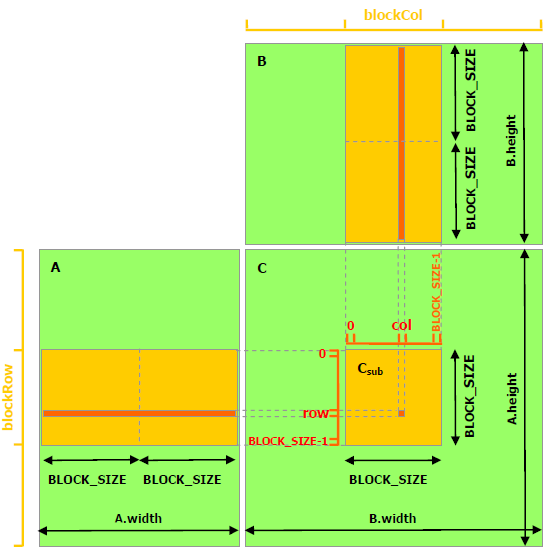
}

// Write Csub to device memory

// Each thread writes one element

SetElement(Csub, row, col, Cvalue);

}

Figure 10. Matrix Multiplication with Shared Memory  
  


### [3.2.4. Page-Locked Host Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "page-locked-host-memory)

The runtime provides functions to allow the use of page-locked (also known as pinned) host memory (as opposed to regular pageable host memory allocated by malloc()):

* cudaHostAlloc() and cudaFreeHost() allocate and free page-locked host memory;
* cudaHostRegister() page-locks a range of memory allocated by malloc() (see reference manual for limitations).

Using page-locked host memory has several benefits:

* Copies between page-locked host memory and device memory can be performed concurrently with kernel execution for some devices as mentioned in [Asynchronous Concurrent Execution](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#asynchronous-concurrent-execution).
* On some devices, page-locked host memory can be mapped into the address space of the device, eliminating the need to copy it to or from device memory as detailed in [Mapped Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#mapped-memory).
* On systems with a front-side bus, bandwidth between host memory and device memory is higher if host memory is allocated as page-locked and even higher if in addition it is allocated as write-combining as described in [Write-Combining Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#write-combining-memory).

Page-locked host memory is a scarce resource however, so allocations in page-locked memory will start failing long before allocations in pageable memory. In addition, by reducing the amount of physical memory available to the operating system for paging, consuming too much page-locked memory reduces overall system performance.

The simple zero-copy CUDA sample comes with a detailed document on the page-locked memory APIs.

### [3.2.4.1. Portable Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "portable-memory)

A block of page-locked memory can be used in conjunction with any device in the system (see [Multi-Device System](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#multi-device-system) for more details on multi-device systems), but by default, the benefits of using page-locked memory described above are only available in conjunction with the device that was current when the block was allocated (and with all devices sharing the same unified address space, if any, as described in [Unified Virtual Address Space](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#unified-virtual-address-space)). To make these advantages available to all devices, the block needs to be allocated by passing the flag cudaHostAllocPortable to cudaHostAlloc() or page-locked by passing the flag cudaHostRegisterPortable to cudaHostRegister().

### [3.2.4.2. Write-Combining Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "write-combining-memory)

By default page-locked host memory is allocated as cacheable. It can optionally be allocated as write-combining instead by passing flag cudaHostAllocWriteCombined to cudaHostAlloc(). Write-combining memory frees up the host's L1 and L2 cache resources, making more cache available to the rest of the application. In addition, write-combining memory is not snooped during transfers across the PCI Express bus, which can improve transfer performance by up to 40%.

Reading from write-combining memory from the host is prohibitively slow, so write-combining memory should in general be used for memory that the host only writes to.

### [3.2.4.3. Mapped Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "mapped-memory)

A block of page-locked host memory can also be mapped into the address space of the device by passing flag cudaHostAllocMapped to cudaHostAlloc() or by passing flag cudaHostRegisterMapped to cudaHostRegister(). Such a block has therefore in general two addresses: one in host memory that is returned by cudaHostAlloc() or malloc(), and one in device memory that can be retrieved using cudaHostGetDevicePointer() and then used to access the block from within a kernel. The only exception is for pointers allocated with cudaHostAlloc() and when a unified address space is used for the host and the device as mentioned in [Unified Virtual Address Space](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#unified-virtual-address-space).

Accessing host memory directly from within a kernel has several advantages:

* There is no need to allocate a block in device memory and copy data between this block and the block in host memory; data transfers are implicitly performed as needed by the kernel;
* There is no need to use streams (see [Concurrent Data Transfers](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#concurrent-data-transfers)) to overlap data transfers with kernel execution; the kernel-originated data transfers automatically overlap with kernel execution.

Since mapped page-locked memory is shared between host and device however, the application must synchronize memory accesses using streams or events (see [Asynchronous Concurrent Execution](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#asynchronous-concurrent-execution)) to avoid any potential read-after-write, write-after-read, or write-after-write hazards.

To be able to retrieve the device pointer to any mapped page-locked memory, page-locked memory mapping must be enabled by calling cudaSetDeviceFlags() with the cudaDeviceMapHost flag before any other CUDA call is performed. Otherwise, cudaHostGetDevicePointer() will return an error.

cudaHostGetDevicePointer() also returns an error if the device does not support mapped page-locked host memory. Applications may query this capability by checking the canMapHostMemory device property (see [Device Enumeration](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#device-enumeration)), which is equal to 1 for devices that support mapped page-locked host memory.

Note that atomic functions (see [Atomic Functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#atomic-functions)) operating on mapped page-locked memory are not atomic from the point of view of the host or other devices.

### [3.2.5. Asynchronous Concurrent Execution](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "asynchronous-concurrent-execution)

### [3.2.5.1. Concurrent Execution between Host and Device](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "concurrent-execution-host-device)

In order to facilitate concurrent execution between host and device, some function calls are asynchronous: Control is returned to the host thread before the device has completed the requested task. These are:

* Kernel launches;
* Memory copies between two addresses to the same device memory;
* Memory copies from host to device of a memory block of 64 KB or less;
* Memory copies performed by functions that are suffixed with Async;
* Memory set function calls.

Programmers can globally disable asynchronous kernel launches for all CUDA applications running on a system by setting the CUDA\_LAUNCH\_BLOCKING environment variable to 1. This feature is provided for debugging purposes only and should never be used as a way to make production software run reliably.

Kernel launches are synchronous if hardware counters are collected via a profiler (Nsight, Visual Profiler).

### [3.2.5.2. Overlap of Data Transfer and Kernel Execution](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "overlap-of-data-transfer-and-kernel-execution)

Some devices can perform copies between page-locked host memory and device memory concurrently with kernel execution. Applications may query this capability by checking the asyncEngineCount device property (see [Device Enumeration](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#device-enumeration)), which is greater than zero for devices that support it.

### [3.2.5.3. Concurrent Kernel Execution](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "concurrent-kernel-execution)

Some devices of compute capability 2.x and higher can execute multiple kernels concurrently. Applications may query this capability by checking the concurrentKernels device property (see [Device Enumeration](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#device-enumeration)), which is equal to 1 for devices that support it.

The maximum number of kernel launches that a device can execute concurrently is 16 on devices of compute capability 2.0 through 3.0; the maximum is 32 concurrent kernel launches on devices of compute capability 3.5 and higher. Devices of compute capability 3.2 are limited to 4 concurrent kernel launches.

A kernel from one CUDA context cannot execute concurrently with a kernel from another CUDA context.

Kernels that use many textures or a large amount of local memory are less likely to execute concurrently with other kernels.

### [3.2.5.4. Concurrent Data Transfers](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "concurrent-data-transfers)

Some devices of compute capability 2.x and higher can perform a copy from page-locked host memory to device memory concurrently with a copy from device memory to page-locked host memory.

Applications may query this capability by checking the asyncEngineCount device property (see [Device Enumeration](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#device-enumeration)), which is equal to 2 for devices that support it.

### [3.2.5.5. Streams](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "streams)

Applications manage concurrency through streams. A stream is a sequence of commands (possibly issued by different host threads) that execute in order. Different streams, on the other hand, may execute their commands out of order with respect to one another or concurrently; this behavior is not guaranteed and should therefore not be relied upon for correctness (e.g., inter-kernel communication is undefined).

### [3.2.5.5.1. Creation and Destruction](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "creation-and-destruction-streams)

A stream is defined by creating a stream object and specifying it as the stream parameter to a sequence of kernel launches and host <-> device memory copies. The following code sample creates two streams and allocates an array hostPtr of float in page-locked memory.

cudaStream\_t stream[2];

for (int i = 0; i < 2; ++i)

cudaStreamCreate(&stream[i]);

float\* hostPtr;

cudaMallocHost(&hostPtr, 2 \* size);

Each of these streams is defined by the following code sample as a sequence of one memory copy from host to device, one kernel launch, and one memory copy from device to host:

for (int i = 0; i < 2; ++i) {

cudaMemcpyAsync(inputDevPtr + i \* size, hostPtr + i \* size,

size, cudaMemcpyHostToDevice, stream[i]);

MyKernel <<<100, 512, 0, stream[i]>>>

(outputDevPtr + i \* size, inputDevPtr + i \* size, size);

cudaMemcpyAsync(hostPtr + i \* size, outputDevPtr + i \* size,

size, cudaMemcpyDeviceToHost, stream[i]);

}

Each stream copies its portion of input array hostPtr to array inputDevPtr in device memory, processes inputDevPtr on the device by calling MyKernel(), and copies the result outputDevPtr back to the same portion of hostPtr. [Overlapping Behavior](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#overlapping-behavior) describes how the streams overlap in this example depending on the capability of the device. Note that hostPtr must point to page-locked host memory for any overlap to occur.

Streams are released by calling cudaStreamDestroy().

for (int i = 0; i < 2; ++i)

cudaStreamDestroy(stream[i]);

cudaStreamDestroy() waits for all preceding commands in the given stream to complete before destroying the stream and returning control to the host thread.

### [3.2.5.5.2. Default Stream](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "default-stream)

Kernel launches and host <-> device memory copies that do not specify any stream parameter, or equivalently that set the stream parameter to zero, are issued to the default stream. They are therefore executed in order.

For code that is compiled using the --default-stream per-thread compilation flag (or that defines the CUDA\_API\_PER\_THREAD\_DEFAULT\_STREAM macro before including CUDA headers (cuda.h and cuda\_runtime.h)), the default stream is a regular stream and each host thread has its own default stream.

For code that is compiled using the --default-stream null compilation flag, the default stream is a special stream called the NULL stream and each device has a single NULL stream used for all host threads. The NULL stream is special as it causes implicit synchronization as described in [Implicit Synchronization](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#implicit-synchronization).

### [3.2.5.5.3. Explicit Synchronization](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "explicit-synchronization)

There are various ways to explicitly synchronize streams with each other.

cudaDeviceSynchronize() waits until all preceding commands in all streams of all host threads have completed.

cudaStreamSynchronize()takes a stream as a parameter and waits until all preceding commands in the given stream have completed. It can be used to synchronize the host with a specific stream, allowing other streams to continue executing on the device.

cudaStreamWaitEvent()takes a stream and an event as parameters (see [Events](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#events) for a description of events)and makes all the commands added to the given stream after the call to cudaStreamWaitEvent()delay their execution until the given event has completed. The stream can be 0, in which case all the commands added to any stream after the call to cudaStreamWaitEvent()wait on the event.

cudaStreamQuery()provides applications with a way to know if all preceding commands in a stream have completed.

To avoid unnecessary slowdowns, all these synchronization functions are usually best used for timing purposes or to isolate a launch or memory copy that is failing.

### [3.2.5.5.4. Implicit Synchronization](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "implicit-synchronization)

Two commands from different streams cannot run concurrently if any one of the following operations is issued in-between them by the host thread:

* a page-locked host memory allocation,
* a device memory allocation,
* a device memory set,
* a memory copy between two addresses to the same device memory,
* any CUDA command to the NULL stream,
* a switch between the L1/shared memory configurations described in [Compute Capability 2.x](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compute-capability-2-x) and [Compute Capability 3.x](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compute-capability-3-0).

For devices that support concurrent kernel execution and are of compute capability 3.0 or lower, any operation that requires a dependency check to see if a streamed kernel launch is complete:

* Can start executing only when all thread blocks of all prior kernel launches from any stream in the CUDA context have started executing;
* Blocks all later kernel launches from any stream in the CUDA context until the kernel launch being checked is complete.

Operations that require a dependency check include any other commands within the same stream as the launch being checked and any call to cudaStreamQuery() on that stream. Therefore, applications should follow these guidelines to improve their potential for concurrent kernel execution:

* All independent operations should be issued before dependent operations,
* Synchronization of any kind should be delayed as long as possible.

### [3.2.5.5.5. Overlapping Behavior](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "overlapping-behavior)

The amount of execution overlap between two streams depends on the order in which the commands are issued to each stream and whether or not the device supports overlap of data transfer and kernel execution (see [Overlap of Data Transfer and Kernel Execution](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#overlap-of-data-transfer-and-kernel-execution)), concurrent kernel execution (see [Concurrent Kernel Execution](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#concurrent-kernel-execution)), and/or concurrent data transfers (see [Concurrent Data Transfers](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#concurrent-data-transfers)).

For example, on devices that do not support concurrent data transfers, the two streams of the code sample of [Creation and Destruction](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#creation-and-destruction-streams) do not overlap at all because the memory copy from host to device is issued to stream[1] after the memory copy from device to host is issued to stream[0], so it can only start once the memory copy from device to host issued to stream[0] has completed. If the code is rewritten the following way (and assuming the device supports overlap of data transfer and kernel execution)

for (int i = 0; i < 2; ++i)

cudaMemcpyAsync(inputDevPtr + i \* size, hostPtr + i \* size,

size, cudaMemcpyHostToDevice, stream[i]);

for (int i = 0; i < 2; ++i)

MyKernel<<<100, 512, 0, stream[i]>>>

(outputDevPtr + i \* size, inputDevPtr + i \* size, size);

for (int i = 0; i < 2; ++i)

cudaMemcpyAsync(hostPtr + i \* size, outputDevPtr + i \* size,

size, cudaMemcpyDeviceToHost, stream[i]);

then the memory copy from host to device issued to stream[1] overlaps with the kernel launch issued to stream[0].

On devices that do support concurrent data transfers, the two streams of the code sample of [Creation and Destruction](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#creation-and-destruction-streams) do overlap: The memory copy from host to device issued to stream[1] overlaps with the memory copy from device to host issued to stream[0] and even with the kernel launch issued to stream[0] (assuming the device supports overlap of data transfer and kernel execution). However, for devices of compute capability 3.0 or lower, the kernel executions cannot possibly overlap because the second kernel launch is issued to stream[1] after the memory copy from device to host is issued to stream[0], so it is blocked until the first kernel launch issued to stream[0] is complete as per [Implicit Synchronization](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#implicit-synchronization). If the code is rewritten as above, the kernel executions overlap (assuming the device supports concurrent kernel execution) since the second kernel launch is issued to stream[1] before the memory copy from device to host is issued to stream[0]. In that case however, the memory copy from device to host issued to stream[0] only overlaps with the last thread blocks of the kernel launch issued to stream[1] as per [Implicit Synchronization](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#implicit-synchronization), which can represent only a small portion of the total execution time of the kernel.

### [3.2.5.5.6. Callbacks](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "stream-callbacks)

The runtime provides a way to insert a callback at any point into a stream via cudaStreamAddCallback(). A callback is a function that is executed on the host once all commands issued to the stream before the callback have completed. Callbacks in stream 0 are executed once all preceding tasks and commands issued in all streams before the callback have completed.

The following code sample adds the callback function MyCallback to each of two streams after issuing a host-to-device memory copy, a kernel launch and a device-to-host memory copy into each stream. The callback will begin execution on the host after each of the device-to-host memory copies completes.

void CUDART\_CB MyCallback(cudaStream\_t stream, cudaError\_t status, void \*data){

printf("Inside callback %d\n", (size\_t)data);

}

...

for (size\_t i = 0; i < 2; ++i) {

cudaMemcpyAsync(devPtrIn[i], hostPtr[i], size, cudaMemcpyHostToDevice, stream[i]);

MyKernel<<<100, 512, 0, stream[i]>>>(devPtrOut[i], devPtrIn[i], size);

cudaMemcpyAsync(hostPtr[i], devPtrOut[i], size, cudaMemcpyDeviceToHost, stream[i]);

cudaStreamAddCallback(stream[i], MyCallback, (void\*)i, 0);

}

The commands that are issued in a stream (or all commands issued to any stream if the callback is issued to stream 0) after a callback do not start executing before the callback has completed. The last parameter of cudaStreamAddCallback() is reserved for future use.

A callback must not make CUDA API calls (directly or indirectly), as it might end up waiting on itself if it makes such a call leading to a deadlock.

### [3.2.5.5.7. Stream Priorities](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "stream-priorities)

The relative priorities of streams can be specified at creation using cudaStreamCreateWithPriority(). The range of allowable priorities, ordered as [ highest priority, lowest priority ] can be obtained using the cudaDeviceGetStreamPriorityRange() function. At runtime, as blocks in low-priority schemes finish, waiting blocks in higher-priority streams are scheduled in their place.

The following code sample obtains the allowable range of priorities for the current device, and creates streams with the highest and lowest available priorities

// get the range of stream priorities for this device

int priority\_high, priority\_low;

cudaDeviceGetStreamPriorityRange(&priority\_low, &priority\_high);

// create streams with highest and lowest available priorities

cudaStream\_t st\_high, st\_low;

cudaStreamCreateWithPriority(&st\_high, cudaStreamNonBlocking, priority\_high);

cudaStreamCreateWithPriority(&st\_low, cudaStreamNonBlocking, priority\_low);

### [3.2.5.6. Events](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "events)

The runtime also provides a way to closely monitor the device's progress, as well as perform accurate timing, by letting the application asynchronously record events at any point in the program and query when these events are completed. An event has completed when all tasks - or optionally, all commands in a given stream - preceding the event have completed. Events in stream zero are completed after all preceding tasks and commands in all streams are completed.

### [3.2.5.6.1. Creation and Destruction](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "creation-and-destruction-events)

The following code sample creates two events:

cudaEvent\_t start, stop;

cudaEventCreate(&start);

cudaEventCreate(&stop);

They are destroyed this way:

cudaEventDestroy(start);

cudaEventDestroy(stop);

### [3.2.5.6.2. Elapsed Time](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "elapsed-time)

The events created in [Creation and Destruction](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#creation-and-destruction-events) can be used to time the code sample of [Creation and Destruction](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#creation-and-destruction-streams) the following way:

cudaEventRecord(start, 0);

for (int i = 0; i < 2; ++i) {

cudaMemcpyAsync(inputDev + i \* size, inputHost + i \* size,

size, cudaMemcpyHostToDevice, stream[i]);

MyKernel<<<100, 512, 0, stream[i]>>>

(outputDev + i \* size, inputDev + i \* size, size);

cudaMemcpyAsync(outputHost + i \* size, outputDev + i \* size,

size, cudaMemcpyDeviceToHost, stream[i]);

}

cudaEventRecord(stop, 0);

cudaEventSynchronize(stop);

float elapsedTime;

cudaEventElapsedTime(&elapsedTime, start, stop);

### [3.2.5.7. Synchronous Calls](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "synchronous-calls)

When a synchronous function is called, control is not returned to the host thread before the device has completed the requested task. Whether the host thread will then yield, block, or spin can be specified by calling cudaSetDeviceFlags()with some specific flags (see reference manual for details) before any other CUDA call is performed by the host thread.

### [3.2.6. Multi-Device System](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "multi-device-system)

### [3.2.6.1. Device Enumeration](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "device-enumeration)

A host system can have multiple devices. The following code sample shows how to enumerate these devices, query their properties, and determine the number of CUDA-enabled devices.

int deviceCount;

cudaGetDeviceCount(&deviceCount);

int device;

for (device = 0; device < deviceCount; ++device) {

cudaDeviceProp deviceProp;

cudaGetDeviceProperties(&deviceProp, device);

printf("Device %d has compute capability %d.%d.\n",

device, deviceProp.major, deviceProp.minor);

}

### [3.2.6.2. Device Selection](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "device-selection)

A host thread can set the device it operates on at any time by calling cudaSetDevice(). Device memory allocations and kernel launches are made on the currently set device; streams and events are created in association with the currently set device. If no call to cudaSetDevice() is made, the current device is device 0.

The following code sample illustrates how setting the current device affects memory allocation and kernel execution.

size\_t size = 1024 \* sizeof(float);

cudaSetDevice(0); // Set device 0 as current

float\* p0;

cudaMalloc(&p0, size); // Allocate memory on device 0

MyKernel<<<1000, 128>>>(p0); // Launch kernel on device 0

cudaSetDevice(1); // Set device 1 as current

float\* p1;

cudaMalloc(&p1, size); // Allocate memory on device 1

MyKernel<<<1000, 128>>>(p1); // Launch kernel on device 1

### [3.2.6.3. Stream and Event Behavior](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "stream-and-event-behavior)

A kernel launch will fail if it is issued to a stream that is not associated to the current device as illustrated in the following code sample.

cudaSetDevice(0); // Set device 0 as current

cudaStream\_t s0;

cudaStreamCreate(&s0); // Create stream s0 on device 0

MyKernel<<<100, 64, 0, s0>>>(); // Launch kernel on device 0 in s0

cudaSetDevice(1); // Set device 1 as current

cudaStream\_t s1;

cudaStreamCreate(&s1); // Create stream s1 on device 1

MyKernel<<<100, 64, 0, s1>>>(); // Launch kernel on device 1 in s1

// This kernel launch will fail:

MyKernel<<<100, 64, 0, s0>>>(); // Launch kernel on device 1 in s0

A memory copy will succeed even if it is issued to a stream that is not associated to the current device.

cudaEventRecord() will fail if the input event and input stream are associated to different devices.

cudaEventElapsedTime() will fail if the two input events are associated to different devices.

cudaEventSynchronize() and cudaEventQuery() will succeed even if the input event is associated to a device that is different from the current device.

cudaStreamWaitEvent() will succeed even if the input stream and input event are associated to different devices. cudaStreamWaitEvent() can therefore be used to synchronize multiple devices with each other.

Each device has its own default stream (see [Default Stream](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#default-stream)), so commands issued to the default stream of a device may execute out of order or concurrently with respect to commands issued to the default stream of any other device.

### [3.2.6.4. Peer-to-Peer Memory Access](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "peer-to-peer-memory-access)

When the application is run as a 64-bit process, devices of compute capability 2.0 and higher from the Tesla series may address each other's memory (i.e., a kernel executing on one device can dereference a pointer to the memory of the other device). This peer-to-peer memory access feature is supported between two devices if cudaDeviceCanAccessPeer() returns true for these two devices.

Peer-to-peer memory access must be enabled between two devices by calling cudaDeviceEnablePeerAccess() as illustrated in the following code sample.

A unified address space is used for both devices (see [Unified Virtual Address Space](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#unified-virtual-address-space)), so the same pointer can be used to address memory from both devices as shown in the code sample below.

cudaSetDevice(0); // Set device 0 as current

float\* p0;

size\_t size = 1024 \* sizeof(float);

cudaMalloc(&p0, size); // Allocate memory on device 0

MyKernel<<<1000, 128>>>(p0); // Launch kernel on device 0

cudaSetDevice(1); // Set device 1 as current

cudaDeviceEnablePeerAccess(0, 0); // Enable peer-to-peer access

// with device 0

// Launch kernel on device 1

// This kernel launch can access memory on device 0 at address p0

MyKernel<<<1000, 128>>>(p0);

### [3.2.6.5. Peer-to-Peer Memory Copy](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "peer-to-peer-memory-copy)

Memory copies can be performed between the memories of two different devices.

When a unified address space is used for both devices (see [Unified Virtual Address Space](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#unified-virtual-address-space)), this is done using the regular memory copy functions mentioned in [Device Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#device-memory).

Otherwise, this is done using cudaMemcpyPeer(), cudaMemcpyPeerAsync(), cudaMemcpy3DPeer(), or cudaMemcpy3DPeerAsync() as illustrated in the following code sample.

cudaSetDevice(0); // Set device 0 as current

float\* p0;

size\_t size = 1024 \* sizeof(float);

cudaMalloc(&p0, size); // Allocate memory on device 0

cudaSetDevice(1); // Set device 1 as current

float\* p1;

cudaMalloc(&p1, size); // Allocate memory on device 1

cudaSetDevice(0); // Set device 0 as current

MyKernel<<<1000, 128>>>(p0); // Launch kernel on device 0

cudaSetDevice(1); // Set device 1 as current

cudaMemcpyPeer(p1, 1, p0, 0, size); // Copy p0 to p1

MyKernel<<<1000, 128>>>(p1); // Launch kernel on device 1

A copy (in the implicit NULL stream) between the memories of two different devices:

* does not start until all commands previously issued to either device have completed and
* runs to completion before any commands (see [Asynchronous Concurrent Execution](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#asynchronous-concurrent-execution)) issued after the copy to either device can start.

Consistent with the normal behavior of streams, an asynchronous copy between the memories of two devices may overlap with copies or kernels in another stream.

Note that if peer-to-peer access is enabled between two devices via cudaDeviceEnablePeerAccess() as described in [Peer-to-Peer Memory Access](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#peer-to-peer-memory-access), peer-to-peer memory copy between these two devices no longer needs to be staged through the host and is therefore faster.

### [3.2.7. Unified Virtual Address Space](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "unified-virtual-address-space)

When the application is run as a 64-bit process, a single address space is used for the host and all the devices of compute capability 2.0 and higher. All host memory allocations made via CUDA API calls and all device memory allocations on supported devices are within this virtual address range. As a consequence:

* The location of any memory on the host allocated through CUDA, or on any of the devices which use the unified address space, can be determined from the value of the pointer using cudaPointerGetAttributes().
* When copying to or from the memory of any device which uses the unified address space, the cudaMemcpyKind parameter of cudaMemcpy\*() can be set to cudaMemcpyDefault to determine locations from the pointers. This also works for host pointers not allocated through CUDA, as long as the current device uses unified addressing.
* Allocations via cudaHostAlloc() are automatically portable (see [Portable Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#portable-memory)) across all the devices for which the unified address space is used, and pointers returned by cudaHostAlloc() can be used directly from within kernels running on these devices (i.e., there is no need to obtain a device pointer via cudaHostGetDevicePointer() as described in [Mapped Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#mapped-memory).

Applications may query if the unified address space is used for a particular device by checking that the unifiedAddressing device property (see [Device Enumeration](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#device-enumeration)) is equal to 1.

### [3.2.8. Interprocess Communication](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "interprocess-communication)

Any device memory pointer or event handle created by a host thread can be directly referenced by any other thread within the same process. It is not valid outside this process however, and therefore cannot be directly referenced by threads belonging to a different process.

To share device memory pointers and events across processes, an application must use the Inter Process Communication API, which is described in detail in the reference manual. The IPC API is only supported for 64-bit processes on Linux and for devices of compute capability 2.0 and higher.

Using this API, an application can get the IPC handle for a given device memory pointer using cudaIpcGetMemHandle(), pass it to another process using standard IPC mechanisms (e.g., interprocess shared memory or files), and use cudaIpcOpenMemHandle() to retrieve a device pointer from the IPC handle that is a valid pointer within this other process. Event handles can be shared using similar entry points.

An example of using the IPC API is where a single master process generates a batch of input data, making the data available to multiple slave processes without requiring regeneration or copying.

### [3.2.9. Error Checking](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "error-checking)

All runtime functions return an error code, but for an asynchronous function (see [Asynchronous Concurrent Execution](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#asynchronous-concurrent-execution)), this error code cannot possibly report any of the asynchronous errors that could occur on the device since the function returns before the device has completed the task; the error code only reports errors that occur on the host prior to executing the task, typically related to parameter validation; if an asynchronous error occurs, it will be reported by some subsequent unrelated runtime function call.

The only way to check for asynchronous errors just after some asynchronous function call is therefore to synchronize just after the call by calling cudaDeviceSynchronize() (or by using any other synchronization mechanisms described in [Asynchronous Concurrent Execution](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#asynchronous-concurrent-execution)) and checking the error code returned by cudaDeviceSynchronize().

The runtime maintains an error variable for each host thread that is initialized to cudaSuccess and is overwritten by the error code every time an error occurs (be it a parameter validation error or an asynchronous error). cudaPeekAtLastError() returns this variable. cudaGetLastError() returns this variable and resets it to cudaSuccess.

Kernel launches do not return any error code, so cudaPeekAtLastError() or cudaGetLastError() must be called just after the kernel launch to retrieve any pre-launch errors. To ensure that any error returned by cudaPeekAtLastError() or cudaGetLastError() does not originate from calls prior to the kernel launch, one has to make sure that the runtime error variable is set to cudaSuccess just before the kernel launch, for example, by calling cudaGetLastError() just before the kernel launch. Kernel launches are asynchronous, so to check for asynchronous errors, the application must synchronize in-between the kernel launch and the call to cudaPeekAtLastError() or cudaGetLastError().

Note that cudaErrorNotReady that may be returned by cudaStreamQuery() and cudaEventQuery() is not considered an error and is therefore not reported by cudaPeekAtLastError() or cudaGetLastError().

### [3.2.10. Call Stack](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "call-stack)

On devices of compute capability 2.x and higher, the size of the call stack can be queried using cudaDeviceGetLimit() and set using cudaDeviceSetLimit().

When the call stack overflows, the kernel call fails with a stack overflow error if the application is run via a CUDA debugger (cuda-gdb, Nsight) or an unspecified launch error, otherwise.

### [3.2.11. Texture and Surface Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "texture-and-surface-memory)

CUDA supports a subset of the texturing hardware that the GPU uses for graphics to access texture and surface memory. Reading data from texture or surface memory instead of global memory can have several performance benefits as described in [Device Memory Accesses](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#device-memory-accesses).

There are two different APIs to access texture and surface memory:

* The texture reference API that is supported on all devices,
* The texture object API that is only supported on devices of compute capability 3.x.

The texture reference API has limitations that the texture object API does not have. They are mentioned in [Texture Reference API](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texture-reference-api).

### [3.2.11.1. Texture Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "texture-memory)

Texture memory is read from kernels using the device functions described in [Texture Functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texture-functions). The process of reading a texture calling one of these functions is called a texture fetch. Each texture fetch specifies a parameter called a texture object for the texture object API or a texture reference for the texture reference API.

The texture object or the texture reference specifies:

* The texture, which is the piece of texture memory that is fetched. Texture objects are created at runtime and the texture is specified when creating the texture object as described in [Texture Object API](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texture-object-api). Texture references are created at compile time and the texture is specified at runtime by bounding the texture reference to the texture through runtime functions as described in [Texture Reference API](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texture-reference-api); several distinct texture references might be bound to the same texture or to textures that overlap in memory. A texture can be any region of linear memory or a CUDA array (described in [CUDA Arrays](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#cuda-arrays)).
* Its dimensionality that specifies whether the texture is addressed as a one dimensional array using one texture coordinate, a two-dimensional array using two texture coordinates, or a three-dimensional array using three texture coordinates. Elements of the array are called texels, short for texture elements. The texture width, height, and depth refer to the size of the array in each dimension. [Table 12](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#features-and-technical-specifications__technical-specifications-per-compute-capability) lists the maximum texture width, height, and depth depending on the compute capability of the device.
* The type of a texel, which is restricted to the basic integer and single-precision floating-point types and any of the 1-, 2-, and 4-component vector types defined in [char, short, int, long, longlong, float, double](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#vector-types) that are derived from the basic integer and single-precision floating-point types.
* The read mode, which is equal to cudaReadModeNormalizedFloat or cudaReadModeElementType. If it is cudaReadModeNormalizedFloat and the type of the texel is a 16-bit or 8-bit integer type, the value returned by the texture fetch is actually returned as floating-point type and the full range of the integer type is mapped to [0.0, 1.0] for unsigned integer type and [-1.0, 1.0] for signed integer type; for example, an unsigned 8-bit texture element with the value 0xff reads as 1. If it is cudaReadModeElementType, no conversion is performed.
* Whether texture coordinates are normalized or not. By default, textures are referenced (by the functions of [Texture Functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texture-functions)) using floating-point coordinates in the range [0, N-1] where N is the size of the texture in the dimension corresponding to the coordinate. For example, a texture that is 64x32 in size will be referenced with coordinates in the range [0, 63] and [0, 31] for the x and y dimensions, respectively. Normalized texture coordinates cause the coordinates to be specified in the range [0.0, 1.0-1/N] instead of [0, N-1], so the same 64x32 texture would be addressed by normalized coordinates in the range [0, 1-1/N] in both the x and y dimensions. Normalized texture coordinates are a natural fit to some applications' requirements, if it is preferable for the texture coordinates to be independent of the texture size.
* The addressing mode. It is valid to call the device functions of Section B.8 with coordinates that are out of range. The addressing mode defines what happens in that case. The default addressing mode is to clamp the coordinates to the valid range: [0, N) for non-normalized coordinates and [0.0, 1.0) for normalized coordinates. If the border mode is specified instead, texture fetches with out-of-range texture coordinates return zero. For normalized coordinates, the warp mode and the mirror mode are also available. When using the wrap mode, each coordinate x is converted to frac(x)=x floor(x) where floor(x) is the largest integer not greater than x. When using the mirror mode, each coordinate x is converted to frac(x) if floor(x) is even and 1-frac(x) if floor(x) is odd. The addressing mode is specified as an array of size three whose first, second, and third elements specify the addressing mode for the first, second, and third texture coordinates, respectively; the addressing mode are cudaAddressModeBorder, cudaAddressModeClamp, cudaAddressModeWrap, and cudaAddressModeMirror; cudaAddressModeWrap and cudaAddressModeMirror are only supported for normalized texture coordinates
* The filtering mode which specifies how the value returned when fetching the texture is computed based on the input texture coordinates. Linear texture filtering may be done only for textures that are configured to return floating-point data. It performs low-precision interpolation between neighboring texels. When enabled, the texels surrounding a texture fetch location are read and the return value of the texture fetch is interpolated based on where the texture coordinates fell between the texels. Simple linear interpolation is performed for one-dimensional textures, bilinear interpolation for two-dimensional textures, and trilinear interpolation for three-dimensional textures. [Texture Fetching](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texture-fetching) gives more details on texture fetching. The filtering mode is equal to cudaFilterModePoint or cudaFilterModeLinear. If it is cudaFilterModePoint, the returned value is the texel whose texture coordinates are the closest to the input texture coordinates. If it is cudaFilterModeLinear, the returned value is the linear interpolation of the two (for a one-dimensional texture), four (for a two dimensional texture), or eight (for a three dimensional texture) texels whose texture coordinates are the closest to the input texture coordinates. cudaFilterModeLinear is only valid for returned values of floating-point type.

[Texture Object API](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texture-object-api) introduces the texture object API.

[Texture Reference API](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texture-reference-api) introduces the texture reference API.

[16-Bit Floating-Point Textures](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#sixteen-bit-floating-point-textures) explains how to deal with 16-bit floating-point textures.

Textures can also be layered as described in [Layered Textures](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#layered-textures).

[Cubemap Textures](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#cubemap-textures) and [Cubemap Layered Textures](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#cubemap-layered-textures) describe a special type of texture, the cubemap texture.

[Texture Gather](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texture-gather) describes a special texture fetch, texture gather.

### [3.2.11.1.1. Texture Object API](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "texture-object-api)

A texture object is created using cudaCreateTextureObject() from a resource description of type struct cudaResourceDesc, which specifies the texture, and from a texture description defined as such:

struct cudaTextureDesc

{

enum cudaTextureAddressMode addressMode[3];

enum cudaTextureFilterMode filterMode;

enum cudaTextureReadMode readMode;

int sRGB;

int normalizedCoords;

unsigned int maxAnisotropy;

enum cudaTextureFilterMode mipmapFilterMode;

float mipmapLevelBias;

float minMipmapLevelClamp;

float maxMipmapLevelClamp;

};

* addressMode specifies the addressing mode;
* filterMode specifies the filter mode;
* readMode specifies the read mode;
* normalizedCoords specifies whether texture coordinates are normalized or not;
* See reference manual for sRGB, maxAnisotropy, mipmapFilterMode, mipmapLevelBias, minMipmapLevelClamp, and maxMipmapLevelClamp.

The following code sample applies some simple transformation kernel to a texture.

// Simple transformation kernel

\_\_global\_\_ void transformKernel(float\* output,

cudaTextureObject\_t texObj,

int width, int height,

float theta)

{

// Calculate normalized texture coordinates

unsigned int x = blockIdx.x \* blockDim.x + threadIdx.x;

unsigned int y = blockIdx.y \* blockDim.y + threadIdx.y;

float u = x / (float)width;

float v = y / (float)height;

// Transform coordinates

u -= 0.5f;

v -= 0.5f;

float tu = u \* cosf(theta) - v \* sinf(theta) + 0.5f;

float tv = v \* cosf(theta) + u \* sinf(theta) + 0.5f;

// Read from texture and write to global memory

output[y \* width + x] = tex2D<float>(texObj, tu, tv);

}

// Host code

int main()

{

// Allocate CUDA array in device memory

cudaChannelFormatDesc channelDesc =

cudaCreateChannelDesc(32, 0, 0, 0,

cudaChannelFormatKindFloat);

cudaArray\* cuArray;

cudaMallocArray(&cuArray, &channelDesc, width, height);

// Copy to device memory some data located at address h\_data

// in host memory

cudaMemcpyToArray(cuArray, 0, 0, h\_data, size,

cudaMemcpyHostToDevice);

// Specify texture

struct cudaResourceDesc resDesc;

memset(&resDesc, 0, sizeof(resDesc));

resDesc.resType = cudaResourceTypeArray;

resDesc.res.array.array = cuArray;

// Specify texture object parameters

struct cudaTextureDesc texDesc;

memset(&texDesc, 0, sizeof(texDesc));

texDesc.addressMode[0] = cudaAddressModeWrap;

texDesc.addressMode[1] = cudaAddressModeWrap;

texDesc.filterMode = cudaFilterModeLinear;

texDesc.readMode = cudaReadModeElementType;

texDesc.normalizedCoords = 1;

// Create texture object

cudaTextureObject\_t texObj = 0;

cudaCreateTextureObject(&texObj, &resDesc, &texDesc, NULL);

// Allocate result of transformation in device memory

float\* output;

cudaMalloc(&output, width \* height \* sizeof(float));

// Invoke kernel

dim3 dimBlock(16, 16);

dim3 dimGrid((width + dimBlock.x - 1) / dimBlock.x,

(height + dimBlock.y - 1) / dimBlock.y);

transformKernel<<<dimGrid, dimBlock>>>(output,

texObj, width, height,

angle);

// Destroy texture object

cudaDestroyTextureObject(texObj);

// Free device memory

cudaFreeArray(cuArray);

cudaFree(output);

return 0;

}

### [3.2.11.1.2. Texture Reference API](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "texture-reference-api)

Some of the attributes of a texture reference are immutable and must be known at compile time; they are specified when declaring the texture reference. A texture reference is declared at file scope as a variable of type texture:

texture<DataType, Type, ReadMode> texRef;

where:

* DataType specifies the type of the texel;
* Type specifies the type of the texture reference and is equal to cudaTextureType1D, cudaTextureType2D, or cudaTextureType3D, for a one-dimensional, two-dimensional, or three-dimensional texture, respectively, or cudaTextureType1DLayered or cudaTextureType2DLayered for a one-dimensional or two-dimensional layered texture respectively; Type is an optional argument which defaults to cudaTextureType1D;
* ReadMode specifies the read mode; it is an optional argument which defaults to cudaReadModeElementType.

A texture reference can only be declared as a static global variable and cannot be passed as an argument to a function.

The other attributes of a texture reference are mutable and can be changed at runtime through the host runtime. As explained in the reference manual, the runtime API has a low-level C-style interface and a high-level C++-style interface. The texture type is defined in the high-level API as a structure publicly derived from the textureReference type defined in the low-level API as such:

struct textureReference {

int normalized;

enum cudaTextureFilterMode filterMode;

enum cudaTextureAddressMode addressMode[3];

struct cudaChannelFormatDesc channelDesc;

int sRGB;

unsigned int maxAnisotropy;

enum cudaTextureFilterMode mipmapFilterMode;

float mipmapLevelBias;

float minMipmapLevelClamp;

float maxMipmapLevelClamp;

}

* normalized specifies whether texture coordinates are normalized or not;
* filterMode specifies the filtering mode;
* addressMode specifies the addressing mode;
* channelDesc describes the format of the texel; it must match the DataType argument of the texture reference declaration; channelDesc is of the following type:
* struct cudaChannelFormatDesc {
* int x, y, z, w;
* enum cudaChannelFormatKind f;

};

where x, y, z, and w are equal to the number of bits of each component of the returned value and f is:

* + cudaChannelFormatKindSigned if these components are of signed integer type,
  + cudaChannelFormatKindUnsigned if they are of unsigned integer type,
  + cudaChannelFormatKindFloat if they are of floating point type.
* See reference manual for sRGB, maxAnisotropy, mipmapFilterMode, mipmapLevelBias, minMipmapLevelClamp, and maxMipmapLevelClamp.

normalized, addressMode, and filterMode may be directly modified in host code.

Before a kernel can use a texture reference to read from texture memory, the texture reference must be bound to a texture using cudaBindTexture() or cudaBindTexture2D() for linear memory, or cudaBindTextureToArray() for CUDA arrays. cudaUnbindTexture() is used to unbind a texture reference. Once a texture reference has been unbound, it can be safely rebound to another array, even if kernels that use the previously bound texture have not completed. It is recommended to allocate two-dimensional textures in linear memory using cudaMallocPitch() and use the pitch returned by cudaMallocPitch() as input parameter to cudaBindTexture2D().

The following code samples bind a 2D texture reference to linear memory pointed to by devPtr:

* Using the low-level API:
* texture<float, cudaTextureType2D,
* cudaReadModeElementType> texRef;
* textureReference\* texRefPtr;
* cudaGetTextureReference(&texRefPtr, &texRef);
* cudaChannelFormatDesc channelDesc =
* cudaCreateChannelDesc<float>();
* size\_t offset;
* cudaBindTexture2D(&offset, texRefPtr, devPtr, &channelDesc,

width, height, pitch);

* Using the high-level API:
* texture<float, cudaTextureType2D,
* cudaReadModeElementType> texRef;
* cudaChannelFormatDesc channelDesc =
* cudaCreateChannelDesc<float>();
* size\_t offset;
* cudaBindTexture2D(&offset, texRef, devPtr, channelDesc,

width, height, pitch);

The following code samples bind a 2D texture reference to a CUDA array cuArray:

* Using the low-level API:
* texture<float, cudaTextureType2D,
* cudaReadModeElementType> texRef;
* textureReference\* texRefPtr;
* cudaGetTextureReference(&texRefPtr, &texRef);
* cudaChannelFormatDesc channelDesc;
* cudaGetChannelDesc(&channelDesc, cuArray);

cudaBindTextureToArray(texRef, cuArray, &channelDesc);

* Using the high-level API:
* texture<float, cudaTextureType2D,
* cudaReadModeElementType> texRef;

cudaBindTextureToArray(texRef, cuArray);

The format specified when binding a texture to a texture reference must match the parameters specified when declaring the texture reference; otherwise, the results of texture fetches are undefined.

There is a limit to the number of textures that can be bound to a kernel as specified in [Table 12](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#features-and-technical-specifications__technical-specifications-per-compute-capability).

The following code sample applies some simple transformation kernel to a texture.

// 2D float texture

texture<float, cudaTextureType2D, cudaReadModeElementType> texRef;

// Simple transformation kernel

\_\_global\_\_ void transformKernel(float\* output,

int width, int height,

float theta)

{

// Calculate normalized texture coordinates

unsigned int x = blockIdx.x \* blockDim.x + threadIdx.x;

unsigned int y = blockIdx.y \* blockDim.y + threadIdx.y;

float u = x / (float)width;

float v = y / (float)height;

// Transform coordinates

u -= 0.5f;

v -= 0.5f;

float tu = u \* cosf(theta) - v \* sinf(theta) + 0.5f;

float tv = v \* cosf(theta) + u \* sinf(theta) + 0.5f;

// Read from texture and write to global memory

output[y \* width + x] = tex2D(texRef, tu, tv);

}

// Host code

int main()

{

// Allocate CUDA array in device memory

cudaChannelFormatDesc channelDesc =

cudaCreateChannelDesc(32, 0, 0, 0,

cudaChannelFormatKindFloat);

cudaArray\* cuArray;

cudaMallocArray(&cuArray, &channelDesc, width, height);

// Copy to device memory some data located at address h\_data

// in host memory

cudaMemcpyToArray(cuArray, 0, 0, h\_data, size,

cudaMemcpyHostToDevice);

// Set texture reference parameters

texRef.addressMode[0] = cudaAddressModeWrap;

texRef.addressMode[1] = cudaAddressModeWrap;

texRef.filterMode = cudaFilterModeLinear;

texRef.normalized = true;

// Bind the array to the texture reference

cudaBindTextureToArray(texRef, cuArray, channelDesc);

// Allocate result of transformation in device memory

float\* output;

cudaMalloc(&output, width \* height \* sizeof(float));

// Invoke kernel

dim3 dimBlock(16, 16);

dim3 dimGrid((width + dimBlock.x - 1) / dimBlock.x,

(height + dimBlock.y - 1) / dimBlock.y);

transformKernel<<<dimGrid, dimBlock>>>(output, width, height,

angle);

// Free device memory

cudaFreeArray(cuArray);

cudaFree(output);

return 0;

}

### [3.2.11.1.3. 16-Bit Floating-Point Textures](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "sixteen-bit-floating-point-textures)

The 16-bit floating-point or half format supported by CUDA arrays is the same as the IEEE 754-2008 binary2 format.

CUDA C does not support a matching data type, but provides intrinsic functions to convert to and from the 32-bit floating-point format via the unsigned short type: \_\_float2half\_rn(float) and \_\_half2float(unsigned short). These functions are only supported in device code. Equivalent functions for the host code can be found in the OpenEXR library, for example.

16-bit floating-point components are promoted to 32 bit float during texture fetching before any filtering is performed.

A channel description for the 16-bit floating-point format can be created by calling one of the cudaCreateChannelDescHalf\*() functions.

### [3.2.11.1.4. Layered Textures](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "layered-textures)

A one-dimensional or two-dimensional layered texture (also known as texture array in Direct3D and array texture in OpenGL) is a texture made up of a sequence of layers, all of which are regular textures of same dimensionality, size, and data type.

A one-dimensional layered texture is addressed using an integer index and a floating-point texture coordinate; the index denotes a layer within the sequence and the coordinate addresses a texel within that layer. A two-dimensional layered texture is addressed using an integer index and two floating-point texture coordinates; the index denotes a layer within the sequence and the coordinates address a texel within that layer.

A layered texture can only be a CUDA array by calling cudaMalloc3DArray() with the cudaArrayLayered flag (and a height of zero for one-dimensional layered texture).

Layered textures are fetched using the device functions described in [tex1DLayered()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#tex1dlayered), [tex1DLayered()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#tex1dlayered-object), [tex2DLayered()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#tex2dlayered), and [tex2DLayered()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#tex2dlayered-object). Texture filtering (see [Texture Fetching](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texture-fetching)) is done only within a layer, not across layers.

Layered textures are only supported on devices of compute capability 2.0 and higher.

### [3.2.11.1.5. Cubemap Textures](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "cubemap-textures)

A cubemap texture is a special type of two-dimensional layered texture that has six layers representing the faces of a cube:

* The width of a layer is equal to its height.
* The cubemap is addressed using three texture coordinates x, y, and z that are interpreted as a direction vector emanating from the center of the cube and pointing to one face of the cube and a texel within the layer corresponding to that face. More specifically, the face is selected by the coordinate with largest magnitude m and the corresponding layer is addressed using coordinates (s/m+1)/2 and (t/m+1)/2 where s and t are defined in [Table 1](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#cubemap-textures__cubemap-fetch).

| Table 1. Cubemap Fetch | | | | | |
| --- | --- | --- | --- | --- | --- |
|  | | **face** | **m** | **s** | **t** |
| |x| > |y| and |x| > |z| | x > 0 | 0 | x | -z | -y |
| x < 0 | 1 | -x | z | -y |
| |y| > |x| and |y| > |z| | y > 0 | 2 | y | x | z |
| y < 0 | 3 | -y | x | -z |
| |z| > |x| and |z| > |y| | z > 0 | 4 | z | x | -y |
| z < 0 | 5 | -z | -x | -y |

A layered texture can only be a CUDA array by calling cudaMalloc3DArray() with the cudaArrayCubemap flag.

Cubemap textures are fetched using the device function described in [texCubemap()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texcubemap) and [texCubemap()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texcubemap-object).

Cubemap textures are only supported on devices of compute capability 2.0 and higher.

### [3.2.11.1.6. Cubemap Layered Textures](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "cubemap-layered-textures)

A cubemap layered texture is a layered texture whose layers are cubemaps of same dimension.

A cubemap layered texture is addressed using an integer index and three floating-point texture coordinates; the index denotes a cubemap within the sequence and the coordinates address a texel within that cubemap.

A layered texture can only be a CUDA array by calling cudaMalloc3DArray() with the cudaArrayLayered and cudaArrayCubemap flags.

Cubemap layered textures are fetched using the device function described in [texCubemapLayered()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texcubemaplayered) and [texCubemapLayered()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texcubemaplayered-object). Texture filtering (see [Texture Fetching](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texture-fetching)) is done only within a layer, not across layers.

Cubemap layered textures are only supported on devices of compute capability 2.0 and higher.

### [3.2.11.1.7. Texture Gather](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "texture-gather)

Texture gather is a special texture fetch that is available for two-dimensional textures only. It is performed by the tex2Dgather() function, which has the same parameters as tex2D(), plus an additional comp parameter equal to 0, 1, 2, or 3 (see [tex2Dgather()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#tex2dgather) and [tex2Dgather()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#tex2dgather-object)). It returns four 32-bit numbers that correspond to the value of the component comp of each of the four texels that would have been used for bilinear filtering during a regular texture fetch. For example, if these texels are of values (253, 20, 31, 255), (250, 25, 29, 254), (249, 16, 37, 253), (251, 22, 30, 250), and comp is 2, tex2Dgather() returns (31, 29, 37, 30).

Texture gather is only supported for CUDA arrays created with the cudaArrayTextureGather flag and of width and height less than the maximum specified in [Table 12](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#features-and-technical-specifications__technical-specifications-per-compute-capability) for texture gather, which is smaller than for regular texture fetch.

Texture gather is only supported on devices of compute capability 2.0 and higher.

### [3.2.11.2. Surface Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "surface-memory)

For devices of compute capability 2.0 and higher, a CUDA array (described in [Cubemap Surfaces](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#cubemap-surfaces)), created with the cudaArraySurfaceLoadStore flag, can be read and written via a surface object or surface reference using the functions described in [Surface Functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#surface-functions).

[Table 12](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#features-and-technical-specifications__technical-specifications-per-compute-capability) lists the maximum surface width, height, and depth depending on the compute capability of the device.

### [3.2.11.2.1. Surface Object API](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "surface-object-api)

A surface object is created using cudaCreateSurfaceObject() from a resource description of type struct cudaResourceDesc.

The following code sample applies some simple transformation kernel to a texture.

// Simple copy kernel

\_\_global\_\_ void copyKernel(cudaSurfaceObject\_t inputSurfObj,

cudaSurfaceObject\_t outputSurfObj,

int width, int height)

{

// Calculate surface coordinates

unsigned int x = blockIdx.x \* blockDim.x + threadIdx.x;

unsigned int y = blockIdx.y \* blockDim.y + threadIdx.y;

if (x < width && y < height) {

uchar4 data;

// Read from input surface

surf2Dread(&data, inputSurfObj, x \* 4, y);

// Write to output surface

surf2Dwrite(data, outputSurfObj, x \* 4, y);

}

}

// Host code

int main()

{

// Allocate CUDA arrays in device memory

cudaChannelFormatDesc channelDesc =

cudaCreateChannelDesc(8, 8, 8, 8,

cudaChannelFormatKindUnsigned);

cudaArray\* cuInputArray;

cudaMallocArray(&cuInputArray, &channelDesc, width, height,

cudaArraySurfaceLoadStore);

cudaArray\* cuOutputArray;

cudaMallocArray(&cuOutputArray, &channelDesc, width, height,

cudaArraySurfaceLoadStore);

// Copy to device memory some data located at address h\_data

// in host memory

cudaMemcpyToArray(cuInputArray, 0, 0, h\_data, size,

cudaMemcpyHostToDevice);

// Specify surface

struct cudaResourceDesc resDesc;

memset(&resDesc, 0, sizeof(resDesc));

resDesc.resType = cudaResourceTypeArray;

// Create the surface objects

resDesc.res.array.array = cuInputArray;

cudaSurfaceObject\_t inputSurfObj = 0;

cudaCreateSurfaceObject(&inputSurfObj, &resDesc);

resDesc.res.array.array = cuOutputArray;

cudaSurfaceObject\_t outputSurfObj = 0;

cudaCreateSurfaceObject(&outputSurfObj, &resDesc);

// Invoke kernel

dim3 dimBlock(16, 16);

dim3 dimGrid((width + dimBlock.x - 1) / dimBlock.x,

(height + dimBlock.y - 1) / dimBlock.y);

copyKernel<<<dimGrid, dimBlock>>>(inputSurfObj,

outputSurfObj,

width, height);

// Destroy surface objects

cudaDestroySurfaceObject(inputSurfObj);

cudaDestroySurfaceObject(outputSurfObj);

// Free device memory

cudaFreeArray(cuInputArray);

cudaFreeArray(cuOutputArray);

return 0;

}

### [3.2.11.2.2. Surface Reference API](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "surface-reference-api)

A surface reference is declared at file scope as a variable of type surface:

surface<void, Type> surfRef;

where Type specifies the type of the surface reference and is equal to cudaSurfaceType1D, cudaSurfaceType2D, cudaSurfaceType3D, cudaSurfaceTypeCubemap, cudaSurfaceType1DLayered, cudaSurfaceType2DLayered, or cudaSurfaceTypeCubemapLayered; Type is an optional argument which defaults to cudaSurfaceType1D. A surface reference can only be declared as a static global variable and cannot be passed as an argument to a function.

Before a kernel can use a surface reference to access a CUDA array, the surface reference must be bound to the CUDA array using cudaBindSurfaceToArray().

The following code samples bind a surface reference to a CUDA array cuArray:

* Using the low-level API:
* surface<void, cudaSurfaceType2D> surfRef;
* surfaceReference\* surfRefPtr;
* cudaGetSurfaceReference(&surfRefPtr, "surfRef");
* cudaChannelFormatDesc channelDesc;
* cudaGetChannelDesc(&channelDesc, cuArray);

cudaBindSurfaceToArray(surfRef, cuArray, &channelDesc);

* Using the high-level API:
* surface<void, cudaSurfaceType2D> surfRef;

cudaBindSurfaceToArray(surfRef, cuArray);

A CUDA array must be read and written using surface functions of matching dimensionality and type and via a surface reference of matching dimensionality; otherwise, the results of reading and writing the CUDA array are undefined.

Unlike texture memory, surface memory uses byte addressing. This means that the x-coordinate used to access a texture element via texture functions needs to be multiplied by the byte size of the element to access the same element via a surface function. For example, the element at texture coordinate x of a one-dimensional floating-point CUDA array bound to a texture reference texRef and a surface reference surfRef is read using tex1d(texRef, x) via texRef, but surf1Dread(surfRef, 4\*x) via surfRef. Similarly, the element at texture coordinate x and y of a two-dimensional floating-point CUDA array bound to a texture reference texRef and a surface reference surfRef is accessed using tex2d(texRef, x, y) via texRef, but surf2Dread(surfRef, 4\*x, y) via surfRef (the byte offset of the y-coordinate is internally calculated from the underlying line pitch of the CUDA array).

The following code sample applies some simple transformation kernel to a texture.

// 2D surfaces

surface<void, 2> inputSurfRef;

surface<void, 2> outputSurfRef;

// Simple copy kernel

\_\_global\_\_ void copyKernel(int width, int height)

{

// Calculate surface coordinates

unsigned int x = blockIdx.x \* blockDim.x + threadIdx.x;

unsigned int y = blockIdx.y \* blockDim.y + threadIdx.y;

if (x < width && y < height) {

uchar4 data;

// Read from input surface

surf2Dread(&data, inputSurfRef, x \* 4, y);

// Write to output surface

surf2Dwrite(data, outputSurfRef, x \* 4, y);

}

}

// Host code

int main()

{

// Allocate CUDA arrays in device memory

cudaChannelFormatDesc channelDesc =

cudaCreateChannelDesc(8, 8, 8, 8,

cudaChannelFormatKindUnsigned);

cudaArray\* cuInputArray;

cudaMallocArray(&cuInputArray, &channelDesc, width, height,

cudaArraySurfaceLoadStore);

cudaArray\* cuOutputArray;

cudaMallocArray(&cuOutputArray, &channelDesc, width, height,

cudaArraySurfaceLoadStore);

// Copy to device memory some data located at address h\_data

// in host memory

cudaMemcpyToArray(cuInputArray, 0, 0, h\_data, size,

cudaMemcpyHostToDevice);

// Bind the arrays to the surface references

cudaBindSurfaceToArray(inputSurfRef, cuInputArray);

cudaBindSurfaceToArray(outputSurfRef, cuOutputArray);

// Invoke kernel

dim3 dimBlock(16, 16);

dim3 dimGrid((width + dimBlock.x - 1) / dimBlock.x,

(height + dimBlock.y - 1) / dimBlock.y);

copyKernel<<<dimGrid, dimBlock>>>(width, height);

// Free device memory

cudaFreeArray(cuInputArray);

cudaFreeArray(cuOutputArray);

return 0;

}

### [3.2.11.2.3. Cubemap Surfaces](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "cubemap-surfaces)

Cubemap surfaces are accessed usingsurfCubemapread() and surfCubemapwrite() ([surfCubemapread](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#surfcubemapread) and [surfCubemapwrite](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#surfcubemapwrite)) as a two-dimensional layered surface, i.e., using an integer index denoting a face and two floating-point texture coordinates addressing a texel within the layer corresponding to this face. Faces are ordered as indicated in [Table 1](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#cubemap-textures__cubemap-fetch).

### [3.2.11.2.4. Cubemap Layered Surfaces](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "cubemap-layered-surfaces)

Cubemap layered surfaces are accessed using surfCubemapLayeredread() and surfCubemapLayeredwrite() ([surfCubemapLayeredread()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#surfcubemaplayeredread) and [surfCubemapLayeredwrite()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#surfcubemaplayeredwrite)) as a two-dimensional layered surface, i.e., using an integer index denoting a face of one of the cubemaps and two floating-point texture coordinates addressing a texel within the layer corresponding to this face. Faces are ordered as indicated in [Table 1](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#cubemap-textures__cubemap-fetch), so index ((2 \* 6) + 3), for example, accesses the fourth face of the third cubemap.

### [3.2.11.3. CUDA Arrays](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "cuda-arrays)

CUDA arrays are opaque memory layouts optimized for texture fetching. They are one dimensional, two dimensional, or three-dimensional and composed of elements, each of which has 1, 2 or 4 components that may be signed or unsigned 8-, 16-, or 32-bit integers, 16-bit floats, or 32-bit floats. CUDA arrays are only accessible by kernels through texture fetching as described in [Texture Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texture-memory) or surface reading and writing as described in [Surface Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#surface-memory).

### [3.2.11.4. Read/Write Coherency](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "read-write-coherency)

The texture and surface memory is cached (see [Device Memory Accesses](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#device-memory-accesses)) and within the same kernel call, the cache is not kept coherent with respect to global memory writes and surface memory writes, so any texture fetch or surface read to an address that has been written to via a global write or a surface write in the same kernel call returns undefined data. In other words, a thread can safely read some texture or surface memory location only if this memory location has been updated by a previous kernel call or memory copy, but not if it has been previously updated by the same thread or another thread from the same kernel call.

### [3.2.12. Graphics Interoperability](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "graphics-interoperability)

Some resources from OpenGL and Direct3D may be mapped into the address space of CUDA, either to enable CUDA to read data written by OpenGL or Direct3D, or to enable CUDA to write data for consumption by OpenGL or Direct3D.

A resource must be registered to CUDA before it can be mapped using the functions mentioned in [OpenGL Interoperability](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#opengl-interoperability) and [Direct3D Interoperability](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#direct3d-interoperability). These functions return a pointer to a CUDA graphics resource of type struct cudaGraphicsResource. Registering a resource is potentially high-overhead and therefore typically called only once per resource. A CUDA graphics resource is unregistered using cudaGraphicsUnregisterResource(). Each CUDA context which intends to use the resource is required to register it separately.

Once a resource is registered to CUDA, it can be mapped and unmapped as many times as necessary using cudaGraphicsMapResources() and cudaGraphicsUnmapResources(). cudaGraphicsResourceSetMapFlags() can be called to specify usage hints (write-only, read-only) that the CUDA driver can use to optimize resource management.

A mapped resource can be read from or written to by kernels using the device memory address returned by cudaGraphicsResourceGetMappedPointer() for buffers and cudaGraphicsSubResourceGetMappedArray() for CUDA arrays.

Accessing a resource through OpenGL, Direct3D, or another CUDA context while it is mapped produces undefined results. [OpenGL Interoperability](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#opengl-interoperability) and [Direct3D Interoperability](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#direct3d-interoperability) give specifics for each graphics API and some code samples. [SLI Interoperability](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#sli-interoperability) gives specifics for when the system is in SLI mode.

### [3.2.12.1. OpenGL Interoperability](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "opengl-interoperability)

The OpenGL resources that may be mapped into the address space of CUDA are OpenGL buffer, texture, and renderbuffer objects.

A buffer object is registered using cudaGraphicsGLRegisterBuffer(). In CUDA, it appears as a device pointer and can therefore be read and written by kernels or via cudaMemcpy() calls.

A texture or renderbuffer object is registered using cudaGraphicsGLRegisterImage(). In CUDA, it appears as a CUDA array. Kernels can read from the array by binding it to a texture or surface reference. They can also write to it via the surface write functions if the resource has been registered with the cudaGraphicsRegisterFlagsSurfaceLoadStore flag. The array can also be read and written via cudaMemcpy2D() calls. cudaGraphicsGLRegisterImage() supports all texture formats with 1, 2, or 4 components and an internal type of float (e.g., GL\_RGBA\_FLOAT32), normalized integer (e.g., GL\_RGBA8, GL\_INTENSITY16), and unnormalized integer (e.g., GL\_RGBA8UI) (please note that since unnormalized integer formats require OpenGL 3.0, they can only be written by shaders, not the fixed function pipeline).

The OpenGL context whose resources are being shared has to be current to the host thread making any OpenGL interoperability API calls.

Please note: When an OpenGL texture is made bindless (say for example by requesting an image or texture handle using the glGetTextureHandle\*/glGetImageHandle\* APIs) it cannot be registered with CUDA. The application needs to register the texture for interop before requesting an image or texture handle.

The following code sample uses a kernel to dynamically modify a 2D width x height grid of vertices stored in a vertex buffer object:

GLuint positionsVBO;

struct cudaGraphicsResource\* positionsVBO\_CUDA;

int main()

{

// Initialize OpenGL and GLUT for device 0

// and make the OpenGL context current

...

glutDisplayFunc(display);

// Explicitly set device 0

cudaSetDevice(0);

// Create buffer object and register it with CUDA

glGenBuffers(1, &positionsVBO);

glBindBuffer(GL\_ARRAY\_BUFFER, positionsVBO);

unsigned int size = width \* height \* 4 \* sizeof(float);

glBufferData(GL\_ARRAY\_BUFFER, size, 0, GL\_DYNAMIC\_DRAW);

glBindBuffer(GL\_ARRAY\_BUFFER, 0);

cudaGraphicsGLRegisterBuffer(&positionsVBO\_CUDA,

positionsVBO,

cudaGraphicsMapFlagsWriteDiscard);

// Launch rendering loop

glutMainLoop();

...

}

void display()

{

// Map buffer object for writing from CUDA

float4\* positions;

cudaGraphicsMapResources(1, &positionsVBO\_CUDA, 0);

size\_t num\_bytes;

cudaGraphicsResourceGetMappedPointer((void\*\*)&positions,

&num\_bytes,

positionsVBO\_CUDA));

// Execute kernel

dim3 dimBlock(16, 16, 1);

dim3 dimGrid(width / dimBlock.x, height / dimBlock.y, 1);

createVertices<<<dimGrid, dimBlock>>>(positions, time,

width, height);

// Unmap buffer object

cudaGraphicsUnmapResources(1, &positionsVBO\_CUDA, 0);

// Render from buffer object

glClear(GL\_COLOR\_BUFFER\_BIT | GL\_DEPTH\_BUFFER\_BIT);

glBindBuffer(GL\_ARRAY\_BUFFER, positionsVBO);

glVertexPointer(4, GL\_FLOAT, 0, 0);

glEnableClientState(GL\_VERTEX\_ARRAY);

glDrawArrays(GL\_POINTS, 0, width \* height);

glDisableClientState(GL\_VERTEX\_ARRAY);

// Swap buffers

glutSwapBuffers();

glutPostRedisplay();

}

void deleteVBO()

{

cudaGraphicsUnregisterResource(positionsVBO\_CUDA);

glDeleteBuffers(1, &positionsVBO);

}

\_\_global\_\_ void createVertices(float4\* positions, float time,

unsigned int width, unsigned int height)

{

unsigned int x = blockIdx.x \* blockDim.x + threadIdx.x;

unsigned int y = blockIdx.y \* blockDim.y + threadIdx.y;

// Calculate uv coordinates

float u = x / (float)width;

float v = y / (float)height;

u = u \* 2.0f - 1.0f;

v = v \* 2.0f - 1.0f;

// calculate simple sine wave pattern

float freq = 4.0f;

float w = sinf(u \* freq + time)

\* cosf(v \* freq + time) \* 0.5f;

// Write positions

positions[y \* width + x] = make\_float4(u, w, v, 1.0f);

}

On Windows and for Quadro GPUs, cudaWGLGetDevice() can be used to retrieve the CUDA device associated to the handle returned by wglEnumGpusNV(). Quadro GPUs offer higher performance OpenGL interoperability than GeForce and Tesla GPUs in a multi-GPU configuration where OpenGL rendering is performed on the Quadro GPU and CUDA computations are performed on other GPUs in the system.

### [3.2.12.2. Direct3D Interoperability](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "direct3d-interoperability)

Direct3D interoperability is supported for Direct3D 9Ex, Direct3D 10, and Direct3D 11.

A CUDA context may interoperate only with Direct3D devices that fulfill the following criteria: Direct3D 9Ex devices must be created with DeviceType set to D3DDEVTYPE\_HAL and BehaviorFlags with the D3DCREATE\_HARDWARE\_VERTEXPROCESSING flag; Direct3D 10 and Direct3D 11 devices must be created with DriverType set to D3D\_DRIVER\_TYPE\_HARDWARE.

The Direct3D resources that may be mapped into the address space of CUDA are Direct3D buffers, textures, and surfaces. These resources are registered using cudaGraphicsD3D9RegisterResource(), cudaGraphicsD3D10RegisterResource(), and cudaGraphicsD3D11RegisterResource().

The following code sample uses a kernel to dynamically modify a 2D width x height grid of vertices stored in a vertex buffer object.

### [3.2.12.2.1. Direct3D 9 Version](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "direct3d-9-version)

IDirect3D9\* D3D;

IDirect3DDevice9\* device;

struct CUSTOMVERTEX {

FLOAT x, y, z;

DWORD color;

};

IDirect3DVertexBuffer9\* positionsVB;

struct cudaGraphicsResource\* positionsVB\_CUDA;

int main()

{

int dev;

// Initialize Direct3D

D3D = Direct3DCreate9Ex(D3D\_SDK\_VERSION);

// Get a CUDA-enabled adapter

unsigned int adapter = 0;

for (; adapter < g\_pD3D->GetAdapterCount(); adapter++) {

D3DADAPTER\_IDENTIFIER9 adapterId;

g\_pD3D->GetAdapterIdentifier(adapter, 0, &adapterId);

int dev;

if (cudaD3D9GetDevice(&dev, adapterId.DeviceName)

== cudaSuccess)

break;

}

// Create device

...

D3D->CreateDeviceEx(adapter, D3DDEVTYPE\_HAL, hWnd,

D3DCREATE\_HARDWARE\_VERTEXPROCESSING,

&params, NULL, &device);

// Use the same device

cudaSetDevice(dev);

// Create vertex buffer and register it with CUDA

unsigned int size = width \* height \* sizeof(CUSTOMVERTEX);

device->CreateVertexBuffer(size, 0, D3DFVF\_CUSTOMVERTEX,

D3DPOOL\_DEFAULT, &positionsVB, 0);

cudaGraphicsD3D9RegisterResource(&positionsVB\_CUDA,

positionsVB,

cudaGraphicsRegisterFlagsNone);

cudaGraphicsResourceSetMapFlags(positionsVB\_CUDA,

cudaGraphicsMapFlagsWriteDiscard);

// Launch rendering loop

while (...) {

...

Render();

...

}

...

}

void Render()

{

// Map vertex buffer for writing from CUDA

float4\* positions;

cudaGraphicsMapResources(1, &positionsVB\_CUDA, 0);

size\_t num\_bytes;

cudaGraphicsResourceGetMappedPointer((void\*\*)&positions,

&num\_bytes,

positionsVB\_CUDA));

// Execute kernel

dim3 dimBlock(16, 16, 1);

dim3 dimGrid(width / dimBlock.x, height / dimBlock.y, 1);

createVertices<<<dimGrid, dimBlock>>>(positions, time,

width, height);

// Unmap vertex buffer

cudaGraphicsUnmapResources(1, &positionsVB\_CUDA, 0);

// Draw and present

...

}

void releaseVB()

{

cudaGraphicsUnregisterResource(positionsVB\_CUDA);

positionsVB->Release();

}

\_\_global\_\_ void createVertices(float4\* positions, float time,

unsigned int width, unsigned int height)

{

unsigned int x = blockIdx.x \* blockDim.x + threadIdx.x;

unsigned int y = blockIdx.y \* blockDim.y + threadIdx.y;

// Calculate uv coordinates

float u = x / (float)width;

float v = y / (float)height;

u = u \* 2.0f - 1.0f;

v = v \* 2.0f - 1.0f;

// Calculate simple sine wave pattern

float freq = 4.0f;

float w = sinf(u \* freq + time)

\* cosf(v \* freq + time) \* 0.5f;

// Write positions

positions[y \* width + x] =

make\_float4(u, w, v, \_\_int\_as\_float(0xff00ff00));

}

### [3.2.12.2.2. Direct3D 10 Version](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "direct3d-10-version)

ID3D10Device\* device;

struct CUSTOMVERTEX {

FLOAT x, y, z;

DWORD color;

};

ID3D10Buffer\* positionsVB;

struct cudaGraphicsResource\* positionsVB\_CUDA;

int main()

{

int dev;

// Get a CUDA-enabled adapter

IDXGIFactory\* factory;

CreateDXGIFactory(\_\_uuidof(IDXGIFactory), (void\*\*)&factory);

IDXGIAdapter\* adapter = 0;

for (unsigned int i = 0; !adapter; ++i) {

if (FAILED(factory->EnumAdapters(i, &adapter))

break;

if (cudaD3D10GetDevice(&dev, adapter) == cudaSuccess)

break;

adapter->Release();

}

factory->Release();

// Create swap chain and device

...

D3D10CreateDeviceAndSwapChain(adapter,

D3D10\_DRIVER\_TYPE\_HARDWARE, 0,

D3D10\_CREATE\_DEVICE\_DEBUG,

D3D10\_SDK\_VERSION,

&swapChainDesc, &swapChain,

&device);

adapter->Release();

// Use the same device

cudaSetDevice(dev);

// Create vertex buffer and register it with CUDA

unsigned int size = width \* height \* sizeof(CUSTOMVERTEX);

D3D10\_BUFFER\_DESC bufferDesc;

bufferDesc.Usage = D3D10\_USAGE\_DEFAULT;

bufferDesc.ByteWidth = size;

bufferDesc.BindFlags = D3D10\_BIND\_VERTEX\_BUFFER;

bufferDesc.CPUAccessFlags = 0;

bufferDesc.MiscFlags = 0;

device->CreateBuffer(&bufferDesc, 0, &positionsVB);

cudaGraphicsD3D10RegisterResource(&positionsVB\_CUDA,

positionsVB,

cudaGraphicsRegisterFlagsNone);

cudaGraphicsResourceSetMapFlags(positionsVB\_CUDA,

cudaGraphicsMapFlagsWriteDiscard);

// Launch rendering loop

while (...) {

...

Render();

...

}

...

}

void Render()

{

// Map vertex buffer for writing from CUDA

float4\* positions;

cudaGraphicsMapResources(1, &positionsVB\_CUDA, 0);

size\_t num\_bytes;

cudaGraphicsResourceGetMappedPointer((void\*\*)&positions,

&num\_bytes,

positionsVB\_CUDA));

// Execute kernel

dim3 dimBlock(16, 16, 1);

dim3 dimGrid(width / dimBlock.x, height / dimBlock.y, 1);

createVertices<<<dimGrid, dimBlock>>>(positions, time,

width, height);

// Unmap vertex buffer

cudaGraphicsUnmapResources(1, &positionsVB\_CUDA, 0);

// Draw and present

...

}

void releaseVB()

{

cudaGraphicsUnregisterResource(positionsVB\_CUDA);

positionsVB->Release();

}

\_\_global\_\_ void createVertices(float4\* positions, float time,

unsigned int width, unsigned int height)

{

unsigned int x = blockIdx.x \* blockDim.x + threadIdx.x;

unsigned int y = blockIdx.y \* blockDim.y + threadIdx.y;

// Calculate uv coordinates

float u = x / (float)width;

float v = y / (float)height;

u = u \* 2.0f - 1.0f;

v = v \* 2.0f - 1.0f;

// Calculate simple sine wave pattern

float freq = 4.0f;

float w = sinf(u \* freq + time)

\* cosf(v \* freq + time) \* 0.5f;

// Write positions

positions[y \* width + x] =

make\_float4(u, w, v, \_\_int\_as\_float(0xff00ff00));

}

### [3.2.12.2.3. Direct3D 11 Version](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "direct3d-11-version)

ID3D11Device\* device;

struct CUSTOMVERTEX {

FLOAT x, y, z;

DWORD color;

};

ID3D11Buffer\* positionsVB;

struct cudaGraphicsResource\* positionsVB\_CUDA;

int main()

{

int dev;

// Get a CUDA-enabled adapter

IDXGIFactory\* factory;

CreateDXGIFactory(\_\_uuidof(IDXGIFactory), (void\*\*)&factory);

IDXGIAdapter\* adapter = 0;

for (unsigned int i = 0; !adapter; ++i) {

if (FAILED(factory->EnumAdapters(i, &adapter))

break;

if (cudaD3D11GetDevice(&dev, adapter) == cudaSuccess)

break;

adapter->Release();

}

factory->Release();

// Create swap chain and device

...

sFnPtr\_D3D11CreateDeviceAndSwapChain(adapter,

D3D11\_DRIVER\_TYPE\_HARDWARE,

0,

D3D11\_CREATE\_DEVICE\_DEBUG,

featureLevels, 3,

D3D11\_SDK\_VERSION,

&swapChainDesc, &swapChain,

&device,

&featureLevel,

&deviceContext);

adapter->Release();

// Use the same device

cudaSetDevice(dev);

// Create vertex buffer and register it with CUDA

unsigned int size = width \* height \* sizeof(CUSTOMVERTEX);

D3D11\_BUFFER\_DESC bufferDesc;

bufferDesc.Usage = D3D11\_USAGE\_DEFAULT;

bufferDesc.ByteWidth = size;

bufferDesc.BindFlags = D3D11\_BIND\_VERTEX\_BUFFER;

bufferDesc.CPUAccessFlags = 0;

bufferDesc.MiscFlags = 0;

device->CreateBuffer(&bufferDesc, 0, &positionsVB);

cudaGraphicsD3D11RegisterResource(&positionsVB\_CUDA,

positionsVB,

cudaGraphicsRegisterFlagsNone);

cudaGraphicsResourceSetMapFlags(positionsVB\_CUDA,

cudaGraphicsMapFlagsWriteDiscard);

// Launch rendering loop

while (...) {

...

Render();

...

}

...

}

void Render()

{

// Map vertex buffer for writing from CUDA

float4\* positions;

cudaGraphicsMapResources(1, &positionsVB\_CUDA, 0);

size\_t num\_bytes;

cudaGraphicsResourceGetMappedPointer((void\*\*)&positions,

&num\_bytes,

positionsVB\_CUDA));

// Execute kernel

dim3 dimBlock(16, 16, 1);

dim3 dimGrid(width / dimBlock.x, height / dimBlock.y, 1);

createVertices<<<dimGrid, dimBlock>>>(positions, time,

width, height);

// Unmap vertex buffer

cudaGraphicsUnmapResources(1, &positionsVB\_CUDA, 0);

// Draw and present

...

}

void releaseVB()

{

cudaGraphicsUnregisterResource(positionsVB\_CUDA);

positionsVB->Release();

}

\_\_global\_\_ void createVertices(float4\* positions, float time,

unsigned int width, unsigned int height)

{

unsigned int x = blockIdx.x \* blockDim.x + threadIdx.x;

unsigned int y = blockIdx.y \* blockDim.y + threadIdx.y;

// Calculate uv coordinates

float u = x / (float)width;

float v = y / (float)height;

u = u \* 2.0f - 1.0f;

v = v \* 2.0f - 1.0f;

// Calculate simple sine wave pattern

float freq = 4.0f;

float w = sinf(u \* freq + time)

\* cosf(v \* freq + time) \* 0.5f;

// Write positions

positions[y \* width + x] =

make\_float4(u, w, v, \_\_int\_as\_float(0xff00ff00));

}

### [3.2.12.3. SLI Interoperability](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "sli-interoperability)

In a system with multiple GPUs, all CUDA-enabled GPUs are accessible via the CUDA driver and runtime as separate devices. There are however special considerations as described below when the system is in SLI mode.

First, an allocation in one CUDA device on one GPU will consume memory on other GPUs that are part of the SLI configuration of the Direct3D or OpenGL device. Because of this, allocations may fail earlier than otherwise expected.

Second, applications should create multiple CUDA contexts, one for each GPU in the SLI configuration. While this is not a strict requirement, it avoids unnecessary data transfers between devices. The application can use the cudaD3D[9|10|11]GetDevices() for Direct3D and cudaGLGetDevices() for OpenGL set of calls to identify the CUDA device handle(s) for the device(s) that are performing the rendering in the current and next frame. Given this information the application will typically choose the appropriate device and map Direct3D or OpenGL resources to the CUDA device returned by cudaD3D[9|10|11]GetDevices() or cudaGLGetDevices() when the deviceList parameter is set to cudaD3D[9|10|11]DeviceListCurrentFrame or cudaGLDeviceListCurrentFrame.

Please note that resource returned from cudaGraphicsD9D[9|10|11]RegisterResource and cudaGraphicsGLRegister[Buffer|Image] must be only used on device the registration happened. Therefore on SLI configurations when data for different frames is computed on different CUDA devices it is necessary to register the resources for each separatly.

See [Direct3D Interoperability](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#direct3d-interoperability) and [OpenGL Interoperability](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#opengl-interoperability) for details on how the CUDA runtime interoperate with Direct3D and OpenGL, respectively.

### [3.3. Versioning and Compatibility](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "versioning-and-compatibility)

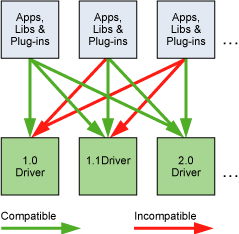
There are two version numbers that developers should care about when developing a CUDA application: The compute capability that describes the general specifications and features of the compute device (see [Compute Capability](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compute-capability)) and the version of the CUDA driver API that describes the features supported by the driver API and runtime.

The version of the driver API is defined in the driver header file as CUDA\_VERSION. It allows developers to check whether their application requires a newer device driver than the one currently installed. This is important, because the driver API is backward compatible, meaning that applications, plug-ins, and libraries (including the C runtime) compiled against a particular version of the driver API will continue to work on subsequent device driver releases as illustrated in [Figure 11](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#versioning-and-compatibility__driver-api-is-backward-but-not-forward-compatible). The driver API is not forward compatible, which means that applications, plug-ins, and libraries (including the C runtime) compiled against a particular version of the driver API will not work on previous versions of the device driver.

It is important to note that there are limitations on the mixing and matching of versions that is supported:

* Since only one version of the CUDA Driver can be installed at a time on a system, the installed driver must be of the same or higher version than the maximum Driver API version against which any application, plug-ins, or libraries that must run on that system were built.
* All plug-ins and libraries used by an application must use the same version of the CUDA Runtime unless they statically link to the Runtime, in which case multiple versions of the runtime can coexist in the same process space. Note that if nvcc is used to link the application, the static version of the CUDA Runtime library will be used by default, and all CUDA Toolkit libraries are statically linked against the CUDA Runtime.
* All plug-ins and libraries used by an application must use the same version of any libraries that use the runtime (such as cuFFT, cuBLAS, ...) unless statically linking to those libraries.

Figure 11. The Driver API Is Backward but Not Forward Compatible



### [3.4. Compute Modes](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "compute-modes)

On Tesla solutions running Windows Server 2008 and later or Linux, one can set any device in a system in one of the three following modes using NVIDIA's System Management Interface (nvidia-smi), which is a tool distributed as part of the driver:

* Default compute mode: Multiple host threads can use the device (by calling cudaSetDevice() on this device, when using the runtime API, or by making current a context associated to the device, when using the driver API) at the same time.
* Exclusive-process compute mode: Only one CUDA context may be created on the device across all processes in the system and that context may be current to as many threads as desired within the process that created that context.
* Exclusive-process-and-thread compute mode: Only one CUDA context may be created on the device across all processes in the system and that context may only be current to one thread at a time.
* Prohibited compute mode: No CUDA context can be created on the device.

This means, in particular, that a host thread using the runtime API without explicitly calling cudaSetDevice() might be associated with a device other than device 0 if device 0 turns out to be in the exclusive-process mode and used by another process, or in the exclusive-process-and-thread mode and used by another thread, or in prohibited mode. cudaSetValidDevices() can be used to set a device from a prioritized list of devices.

Applications may query the compute mode of a device by checking the computeMode device property (see [Device Enumeration](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#device-enumeration)).

### [3.5. Mode Switches](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "mode-switches)

GPUs that have a display output dedicate some DRAM memory to the so-called primary surface, which is used to refresh the display device whose output is viewed by the user. When users initiate a mode switch of the display by changing the resolution or bit depth of the display (using NVIDIA control panel or the Display control panel on Windows), the amount of memory needed for the primary surface changes. For example, if the user changes the display resolution from 1280x1024x32-bit to 1600x1200x32-bit, the system must dedicate 7.68 MB to the primary surface rather than 5.24 MB. (Full-screen graphics applications running with anti-aliasing enabled may require much more display memory for the primary surface.) On Windows, other events that may initiate display mode switches include launching a full-screen DirectX application, hitting Alt+Tab to task switch away from a full-screen DirectX application, or hitting Ctrl+Alt+Del to lock the computer.

If a mode switch increases the amount of memory needed for the primary surface, the system may have to cannibalize memory allocations dedicated to CUDA applications. Therefore, a mode switch results in any call to the CUDA runtime to fail and return an invalid context error.

### [3.6. Tesla Compute Cluster Mode for Windows](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "tesla-compute-cluster-mode-for-windows)

Using NVIDIA's System Management Interface (nvidia-smi), the Windows device driver can be put in TCC (Tesla Compute Cluster) mode for devices of the Tesla and Quadro Series of compute capability 2.0 and higher.

This mode has the following primary benefits:

* It makes it possible to use these GPUs in cluster nodes with non-NVIDIA integrated graphics;
* It makes these GPUs available via Remote Desktop, both directly and via cluster management systems that rely on Remote Desktop;
* It makes these GPUs available to applications running as a Windows service (i.e., in Session 0).

However, the TCC mode removes support for any graphics functionality.

## [4. Hardware Implementation](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "hardware-implementation)

The NVIDIA GPU architecture is built around a scalable array of multithreaded Streaming Multiprocessors (SMs). When a CUDA program on the host CPU invokes a kernel grid, the blocks of the grid are enumerated and distributed to multiprocessors with available execution capacity. The threads of a thread block execute concurrently on one multiprocessor, and multiple thread blocks can execute concurrently on one multiprocessor. As thread blocks terminate, new blocks are launched on the vacated multiprocessors.

A multiprocessor is designed to execute hundreds of threads concurrently. To manage such a large amount of threads, it employs a unique architecture called SIMT (Single-Instruction, Multiple-Thread) that is described in [SIMT Architecture](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#simt-architecture). The instructions are pipelined to leverage instruction-level parallelism within a single thread, as well as thread-level parallelism extensively through simultaneous hardware multithreading as detailed in [Hardware Multithreading](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#hardware-multithreading). Unlike CPU cores they are issued in order however and there is no branch prediction and no speculative execution.

[SIMT Architecture](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#simt-architecture) and [Hardware Multithreading](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#hardware-multithreading) describe the architecture features of the streaming multiprocessor that are common to all devices. [Compute Capability 2.x](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compute-capability-2-x), [Compute Capability 3.x](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compute-capability-3-0), and [Compute Capability 5.x](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compute-capability-5-x) provide the specifics for devices of compute capabilities 2.x, 3.x, and 5.x, respectively.

The NVIDIA GPU architecture uses a little-endian representation.

### [4.1. SIMT Architecture](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "simt-architecture)

The multiprocessor creates, manages, schedules, and executes threads in groups of 32 parallel threads called warps. Individual threads composing a warp start together at the same program address, but they have their own instruction address counter and register state and are therefore free to branch and execute independently. The term warp originates from weaving, the first parallel thread technology. A half-warp is either the first or second half of a warp. A quarter-warp is either the first, second, third, or fourth quarter of a warp.

When a multiprocessor is given one or more thread blocks to execute, it partitions them into warps and each warp gets scheduled by a warp scheduler for execution. The way a block is partitioned into warps is always the same; each warp contains threads of consecutive, increasing thread IDs with the first warp containing thread 0. [Thread Hierarchy](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#thread-hierarchy) describes how thread IDs relate to thread indices in the block.

A warp executes one common instruction at a time, so full efficiency is realized when all 32 threads of a warp agree on their execution path. If threads of a warp diverge via a data-dependent conditional branch, the warp serially executes each branch path taken, disabling threads that are not on that path, and when all paths complete, the threads converge back to the same execution path. Branch divergence occurs only within a warp; different warps execute independently regardless of whether they are executing common or disjoint code paths.

The SIMT architecture is akin to SIMD (Single Instruction, Multiple Data) vector organizations in that a single instruction controls multiple processing elements. A key difference is that SIMD vector organizations expose the SIMD width to the software, whereas SIMT instructions specify the execution and branching behavior of a single thread. In contrast with SIMD vector machines, SIMT enables programmers to write thread-level parallel code for independent, scalar threads, as well as data-parallel code for coordinated threads. For the purposes of correctness, the programmer can essentially ignore the SIMT behavior; however, substantial performance improvements can be realized by taking care that the code seldom requires threads in a warp to diverge. In practice, this is analogous to the role of cache lines in traditional code: Cache line size can be safely ignored when designing for correctness but must be considered in the code structure when designing for peak performance. Vector architectures, on the other hand, require the software to coalesce loads into vectors and manage divergence manually.

### Notes

The threads of a warp that are on that warp's current execution path are called the active threads, whereas threads not on the current path are inactive (disabled). Threads can be inactive because they have exited earlier than other threads of their warp, or because they are on a different branch path than the branch path currently executed by the warp, or because they are the last threads of a block whose number of threads is not a multiple of the warp size.

If a non-atomic instruction executed by a warp writes to the same location in global or shared memory for more than one of the threads of the warp, the number of serialized writes that occur to that location varies depending on the compute capability of the device (see [Compute Capability 2.x](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compute-capability-2-x), [Compute Capability 3.x](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compute-capability-3-0), and [Compute Capability 5.x](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compute-capability-5-x)), and which thread performs the final write is undefined.

If an [atomic](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#atomic-functions) instruction executed by a warp reads, modifies, and writes to the same location in global memory for more than one of the threads of the warp, each read/modify/write to that location occurs and they are all serialized, but the order in which they occur is undefined.

### [4.2. Hardware Multithreading](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "hardware-multithreading)

The execution context (program counters, registers, etc.) for each warp processed by a multiprocessor is maintained on-chip during the entire lifetime of the warp. Therefore, switching from one execution context to another has no cost, and at every instruction issue time, a warp scheduler selects a warp that has threads ready to execute its next instruction (the [active threads](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#simt-architecture__notes) of the warp) and issues the instruction to those threads.

In particular, each multiprocessor has a set of 32-bit registers that are partitioned among the warps, and a parallel data cache or shared memory that is partitioned among the thread blocks.

The number of blocks and warps that can reside and be processed together on the multiprocessor for a given kernel depends on the amount of registers and shared memory used by the kernel and the amount of registers and shared memory available on the multiprocessor. There are also a maximum number of resident blocks and a maximum number of resident warps per multiprocessor. These limits as well the amount of registers and shared memory available on the multiprocessor are a function of the compute capability of the device and are given in Appendix [Compute Capabilities](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compute-capabilities). If there are not enough registers or shared memory available per multiprocessor to process at least one block, the kernel will fail to launch.

The total number of warps in a block is as follows:

ceil ( T W s i z e , 1 )

* T is the number of threads per block,
* Wsize is the warp size, which is equal to 32,
* ceil(x, y) is equal to x rounded up to the nearest multiple of y.

The total number of registers and total amount of shared memory allocated for a block are documented in the CUDA Occupancy Calculator provided in the CUDA Toolkit.

## [5. Performance Guidelines](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "performance-guidelines)

### [5.1. Overall Performance Optimization Strategies](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "overall-performance-optimization-strategies)

Performance optimization revolves around three basic strategies:

* Maximize parallel execution to achieve maximum utilization;
* Optimize memory usage to achieve maximum memory throughput;
* Optimize instruction usage to achieve maximum instruction throughput.

Which strategies will yield the best performance gain for a particular portion of an application depends on the performance limiters for that portion; optimizing instruction usage of a kernel that is mostly limited by memory accesses will not yield any significant performance gain, for example. Optimization efforts should therefore be constantly directed by measuring and monitoring the performance limiters, for example using the CUDA profiler. Also, comparing the floating-point operation throughput or memory throughput - whichever makes more sense - of a particular kernel to the corresponding peak theoretical throughput of the device indicates how much room for improvement there is for the kernel.

### [5.2. Maximize Utilization](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "maximize-utilization)

To maximize utilization the application should be structured in a way that it exposes as much parallelism as possible and efficiently maps this parallelism to the various components of the system to keep them busy most of the time.

### [5.2.1. Application Level](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "application-level)

At a high level, the application should maximize parallel execution between the host, the devices, and the bus connecting the host to the devices, by using asynchronous functions calls and streams as described in [Asynchronous Concurrent Execution](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#asynchronous-concurrent-execution). It should assign to each processor the type of work it does best: serial workloads to the host; parallel workloads to the devices.

For the parallel workloads, at points in the algorithm where parallelism is broken because some threads need to synchronize in order to share data with each other, there are two cases: Either these threads belong to the same block, in which case they should use \_\_syncthreads() and share data through shared memory within the same kernel invocation, or they belong to different blocks, in which case they must share data through global memory using two separate kernel invocations, one for writing to and one for reading from global memory. The second case is much less optimal since it adds the overhead of extra kernel invocations and global memory traffic. Its occurrence should therefore be minimized by mapping the algorithm to the CUDA programming model in such a way that the computations that require inter-thread communication are performed within a single thread block as much as possible.

### [5.2.2. Device Level](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "device-level)

At a lower level, the application should maximize parallel execution between the multiprocessors of a device.

Multiple kernels can execute concurrently on a device, so maximum utilization can also be achieved by using streams to enable enough kernels to execute concurrently as described in [Asynchronous Concurrent Execution](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#asynchronous-concurrent-execution).

### [5.2.3. Multiprocessor Level](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "multiprocessor-level)

At an even lower level, the application should maximize parallel execution between the various functional units within a multiprocessor.

As described in [Hardware Multithreading](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#hardware-multithreading), a GPU multiprocessor relies on thread-level parallelism to maximize utilization of its functional units. Utilization is therefore directly linked to the number of resident warps. At every instruction issue time, a warp scheduler selects a warp that is ready to execute its next instruction, if any, and issues the instruction to the [active](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#simt-architecture__notes) threads of the warp. The number of clock cycles it takes for a warp to be ready to execute its next instruction is called the latency, and full utilization is achieved when all warp schedulers always have some instruction to issue for some warp at every clock cycle during that latency period, or in other words, when latency is completely "hidden". The number of instructions required to hide a latency of L clock cycles depends on the respective throughputs of these instructions (see [Arithmetic Instructions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#arithmetic-instructions) for the throughputs of various arithmetic instructions); assuming maximum throughput for all instructions, it is:

* L for devices of compute capability 2.0 since a multiprocessor issues one instruction per warp over two clock cycles for two warps at a time, as mentioned in [Compute Capability 2.x](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compute-capability-2-x),
* 2L for devices of compute capability 2.1 since a multiprocessor issues a pair of instructions per warp over two clock cycles for two warps at a time, as mentioned in [Compute Capability 2.x](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compute-capability-2-x),
* 8L for devices of compute capability 3.x since a multiprocessor issues a pair of instructions per warp over one clock cycle for four warps at a time, as mentioned in [Compute Capability 3.x](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compute-capability-3-0).

For devices of compute capability 2.0, the two instructions issued every other cycle are for two different warps. For devices of compute capability 2.1, the four instructions issued every other cycle are two pairs for two different warps, each pair being for the same warp.

For devices of compute capability 3.x, the eight instructions issued every cycle are four pairs for four different warps, each pair being for the same warp.

The most common reason a warp is not ready to execute its next instruction is that the instruction's input operands are not available yet.

If all input operands are registers, latency is caused by register dependencies, i.e., some of the input operands are written by some previous instruction(s) whose execution has not completed yet. In the case of a back-to-back register dependency (i.e., some input operand is written by the previous instruction), the latency is equal to the execution time of the previous instruction and the warp schedulers must schedule instructions for different warps during that time. Execution time varies depending on the instruction, but it is typically about 22 clock cycles for devices of compute capability 2.x and about 11 clock cycles for devices of compute capability 3.x, which translates to 22 warps for devices of compute capability 2.x and 44 warps for devices of compute capability 3.x and higher (still assuming that warps execute instructions with maximum throughput, otherwise fewer warps are needed). For devices of compute capability 2.1 and higher, this is also assuming enough instruction-level parallelism so that schedulers are always able to issue pairs of instructions for each warp.

If some input operand resides in off-chip memory, the latency is much higher: 400 to 800 clock cycles for devices of compute capability 2.x and about 200 to 400 clock cycles for devices of compute capability 3.x. The number of warps required to keep the warp schedulers busy during such high latency periods depends on the kernel code and its degree of instruction-level parallelism. In general, more warps are required if the ratio of the number of instructions with no off-chip memory operands (i.e., arithmetic instructions most of the time) to the number of instructions with off-chip memory operands is low (this ratio is commonly called the arithmetic intensity of the program). For example, assume this ratio is 30, also assume the latencies are 600 cycles on devices of compute capability 2.x and 300 cycles on devices of compute capability 3.x. Then about 20 warps are required for devices of compute capability 2.x and about 40 for devices of compute capability 3.x (with the same assumptions as in the previous paragraph).

Another reason a warp is not ready to execute its next instruction is that it is waiting at some memory fence ([Memory Fence Functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#memory-fence-functions)) or synchronization point ([Memory Fence Functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#memory-fence-functions)). A synchronization point can force the multiprocessor to idle as more and more warps wait for other warps in the same block to complete execution of instructions prior to the synchronization point. Having multiple resident blocks per multiprocessor can help reduce idling in this case, as warps from different blocks do not need to wait for each other at synchronization points.

The number of blocks and warps residing on each multiprocessor for a given kernel call depends on the execution configuration of the call ([Execution Configuration](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#execution-configuration)), the memory resources of the multiprocessor, and the resource requirements of the kernel as described in [Hardware Multithreading](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#hardware-multithreading). Register and shared memory usage are reported by the compiler when compiling with the -ptxas-options=-v option.

The total amount of shared memory required for a block is equal to the sum of the amount of statically allocated shared memory and the amount of dynamically allocated shared memory.

The number of registers used by a kernel can have a significant impact on the number of resident warps. For example, for devices of compute capability 2.x, if a kernel uses 32 registers and each block has 512 threads and requires very little shared memory, then two blocks (i.e., 32 warps) can reside on the multiprocessor since they require 2x512x32 registers, which exactly matches the number of registers available on the multiprocessor. But as soon as the kernel uses one more register, only one block (i.e., 16 warps) can be resident since two blocks would require 2x512x17 registers, which are more registers than are available on the multiprocessor. Therefore, the compiler attempts to minimize register usage while keeping register spilling (see [Device Memory Accesses](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#device-memory-accesses)) and the number of instructions to a minimum. Register usage can be controlled using the maxrregcount compiler option or launch bounds as described in [Launch Bounds](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#launch-bounds).

Each double variable and each long long variable uses two registers.

The effect of execution configuration on performance for a given kernel call generally depends on the kernel code. Experimentation is therefore recommended. Applications can also parameterize execution configurations based on register file size and shared memory size, which depends on the compute capability of the device, as well as on the number of multiprocessors and memory bandwidth of the device, all of which can be queried using the runtime (see reference manual).

The number of threads per block should be chosen as a multiple of the warp size to avoid wasting computing resources with under-populated warps as much as possible.

### [5.2.3.1. Occupancy Calculator](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "occupancy-calculator)

Several API functions exist to assist programmers in choosing thread block size based on register and shared memory requirements.

* The occupancy calculator API, cudaOccupancyMaxActiveBlocksPerMultiprocessor, can provide an occupancy prediction based on the block size and shared memory usage of a kernel. This function reports occupancy in terms of the number of concurrent thread blocks per multiprocessor.
  + Note that this value can be converted to other metrics. Multiplying by the number of warps per block yields the number of concurrent warps per multiprocessor; further dividing concurrent warps by max warps per multiprocessor gives the occupancy as a percentage.
* The occupancy-based launch configurator APIs, cudaOccupancyMaxPotentialBlockSize and cudaOccupancyMaxPotentialBlockSizeVariableSMem, heuristically calculate an execution configuration that achieves the maximum multiprocessor-level occupancy.

The following code sample calculates the occupancy of MyKernel. It then reports the occupancy level with the ratio between concurrent warps versus maximum warps per multiprocessor.

// Device code

\_\_global\_\_ void MyKernel(int \*d, int \*a, int \*b)

{

int idx = threadIdx.x + blockIdx.x \* blockDim.x;

d[idx] = a[idx] \* b[idx];

}

// Host code

int main()

{

int numBlocks; // Occupancy in terms of active blocks

int blockSize = 32;

// These variables are used to convert occupancy to warps

int device;

cudaDeviceProp prop;

int activeWarps;

int maxWarps;

cudaGetDevice(&device);

cudaGetDeviceProperties(&prop, device);

cudaOccupancyMaxActiveBlocksPerMultiprocessor(

&numBlocks,

MyKernel,

blockSize,

0);

activeWarps = numBlocks \* blockSize / prop.warpSize;

maxWarps = prop.maxThreadsPerMultiProcessor / prop.warpSize;

std::cout << "Occupancy: " << (double)activeWarps / maxWarps \* 100 << "%" << std::endl;

return 0;

}

The following code sample configures an occupancy-based kernel launch of MyKernel according to the user input.

// Device code

\_\_global\_\_ void MyKernel(int \*array, int arrayCount)

{

int idx = threadIdx.x + blockIdx.x \* blockDim.x;

if (idx < arrayCount) {

array[idx] \*= array[idx];

}

}

// Host code

int launchMyKernel(int \*array, int arrayCount)

{

int blockSize; // The launch configurator returned block size

int minGridSize; // The minimum grid size needed to achieve the

// maximum occupancy for a full device

// launch

int gridSize; // The actual grid size needed, based on input

// size

cudaOccupancyMaxPotentialBlockSize(

&minGridSize,

&blockSize,

(void\*)MyKernel,

0,

arrayCount);

// Round up according to array size

gridSize = (arrayCount + blockSize - 1) / blockSize;

MyKernel<<<gridSize, blockSize>>>(array, arrayCount);

cudaDeviceSynchronize();

// If interested, the occupancy can be calculated with

// cudaOccupancyMaxActiveBlocksPerMultiprocessor

return 0;

}

The CUDA Toolkit also provides a self-documenting, standalone occupancy calculator and launch configurator implementation in <CUDA\_Toolkit\_Path>/include/cuda\_occupancy.h for any use cases that cannot depend on the CUDA software stack. A spreadsheet version of the occupancy calculator is also provided. The spreadsheet version is particularly useful as a learning tool that visualizes the impact of changes to the parameters that affect occupancy (block size, registers per thread, and shared memory per thread).

### [5.3. Maximize Memory Throughput](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "maximize-memory-throughput)

The first step in maximizing overall memory throughput for the application is to minimize data transfers with low bandwidth.

That means minimizing data transfers between the host and the device, as detailed in [Data Transfer between Host and Device](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#data-transfer-between-host-and-device), since these have much lower bandwidth than data transfers between global memory and the device.

That also means minimizing data transfers between global memory and the device by maximizing use of on-chip memory: shared memory and caches (i.e., L1 cache available on devices of compute capability 2.x and 3.x, L2 cache available on devices of compute capability 2.x and higher, texture cache and constant cache available on all devices).

Shared memory is equivalent to a user-managed cache: The application explicitly allocates and accesses it. As illustrated in [CUDA C Runtime](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#cuda-c-runtime), a typical programming pattern is to stage data coming from device memory into shared memory; in other words, to have each thread of a block:

* Load data from device memory to shared memory,
* Synchronize with all the other threads of the block so that each thread can safely read shared memory locations that were populated by different threads,
* Process the data in shared memory,
* Synchronize again if necessary to make sure that shared memory has been updated with the results,
* Write the results back to device memory.

For some applications (e.g., for which global memory access patterns are data-dependent), a traditional hardware-managed cache is more appropriate to exploit data locality. As mentioned in [Compute Capability 2.x](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compute-capability-2-x) and [Compute Capability 3.x](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compute-capability-3-0), for devices of compute capability 2.x and 3.x, the same on-chip memory is used for both L1 and shared memory, and how much of it is dedicated to L1 versus shared memory is configurable for each kernel call.

The throughput of memory accesses by a kernel can vary by an order of magnitude depending on access pattern for each type of memory. The next step in maximizing memory throughput is therefore to organize memory accesses as optimally as possible based on the optimal memory access patterns described in [Device Memory Accesses](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#device-memory-accesses). This optimization is especially important for global memory accesses as global memory bandwidth is low, so non-optimal global memory accesses have a higher impact on performance.

### [5.3.1. Data Transfer between Host and Device](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "data-transfer-between-host-and-device)

Applications should strive to minimize data transfer between the host and the device. One way to accomplish this is to move more code from the host to the device, even if that means running kernels with low parallelism computations. Intermediate data structures may be created in device memory, operated on by the device, and destroyed without ever being mapped by the host or copied to host memory.

Also, because of the overhead associated with each transfer, batching many small transfers into a single large transfer always performs better than making each transfer separately.

On systems with a front-side bus, higher performance for data transfers between host and device is achieved by using page-locked host memory as described in [Page-Locked Host Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#page-locked-host-memory).

In addition, when using mapped page-locked memory ([Mapped Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#mapped-memory)), there is no need to allocate any device memory and explicitly copy data between device and host memory. Data transfers are implicitly performed each time the kernel accesses the mapped memory. For maximum performance, these memory accesses must be coalesced as with accesses to global memory (see [Device Memory Accesses](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#device-memory-accesses)). Assuming that they are and that the mapped memory is read or written only once, using mapped page-locked memory instead of explicit copies between device and host memory can be a win for performance.

On integrated systems where device memory and host memory are physically the same, any copy between host and device memory is superfluous and mapped page-locked memory should be used instead. Applications may query a device is integrated by checking that the integrated device property (see [Device Enumeration](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#device-enumeration)) is equal to 1.

### [5.3.2. Device Memory Accesses](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "device-memory-accesses)

An instruction that accesses addressable memory (i.e., global, local, shared, constant, or texture memory) might need to be re-issued multiple times depending on the distribution of the memory addresses across the threads within the warp. How the distribution affects the instruction throughput this way is specific to each type of memory and described in the following sections. For example, for global memory, as a general rule, the more scattered the addresses are, the more reduced the throughput is.

#### Global Memory

Global memory resides in device memory and device memory is accessed via 32-, 64-, or 128-byte memory transactions. These memory transactions must be naturally aligned: Only the 32-, 64-, or 128-byte segments of device memory that are aligned to their size (i.e., whose first address is a multiple of their size) can be read or written by memory transactions.

When a warp executes an instruction that accesses global memory, it coalesces the memory accesses of the threads within the warp into one or more of these memory transactions depending on the size of the word accessed by each thread and the distribution of the memory addresses across the threads. In general, the more transactions are necessary, the more unused words are transferred in addition to the words accessed by the threads, reducing the instruction throughput accordingly. For example, if a 32-byte memory transaction is generated for each thread's 4-byte access, throughput is divided by 8.

How many transactions are necessary and how much throughput is ultimately affected varies with the compute capability of the device. [Compute Capability 2.x](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compute-capability-2-x), [Compute Capability 3.x](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compute-capability-3-0), and [Compute Capability 5.x](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compute-capability-5-x) give more details on how global memory accesses are handled for various compute capabilities.

To maximize global memory throughput, it is therefore important to maximize coalescing by:

* Following the most optimal access patterns based on [Compute Capability 2.x](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compute-capability-2-x) and [Compute Capability 3.x](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compute-capability-3-0),
* Using data types that meet the size and alignment requirement detailed in [Device Memory Accesses](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#device-memory-accesses),
* Padding data in some cases, for example, when accessing a two-dimensional array as described in [Device Memory Accesses](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#device-memory-accesses).

#### Size and Alignment Requirement

Global memory instructions support reading or writing words of size equal to 1, 2, 4, 8, or 16 bytes. Any access (via a variable or a pointer) to data residing in global memory compiles to a single global memory instruction if and only if the size of the data type is 1, 2, 4, 8, or 16 bytes and the data is naturally aligned (i.e., its address is a multiple of that size).

If this size and alignment requirement is not fulfilled, the access compiles to multiple instructions with interleaved access patterns that prevent these instructions from fully coalescing. It is therefore recommended to use types that meet this requirement for data that resides in global memory.

The alignment requirement is automatically fulfilled for the built-in types of [char, short, int, long, longlong, float, double](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#vector-types) like float2 or float4.

For structures, the size and alignment requirements can be enforced by the compiler using the alignment specifiers \_\_align\_\_(8) or \_\_align\_\_(16), such as

struct \_\_align\_\_(8) {

float x;

float y;

};

or

struct \_\_align\_\_(16) {

float x;

float y;

float z;

};

Any address of a variable residing in global memory or returned by one of the memory allocation routines from the driver or runtime API is always aligned to at least 256 bytes.

Reading non-naturally aligned 8-byte or 16-byte words produces incorrect results (off by a few words), so special care must be taken to maintain alignment of the starting address of any value or array of values of these types. A typical case where this might be easily overlooked is when using some custom global memory allocation scheme, whereby the allocations of multiple arrays (with multiple calls to cudaMalloc() or cuMemAlloc()) is replaced by the allocation of a single large block of memory partitioned into multiple arrays, in which case the starting address of each array is offset from the block's starting address.

#### Two-Dimensional Arrays

A common global memory access pattern is when each thread of index (tx,ty) uses the following address to access one element of a 2D array of width width, located at address BaseAddress of type type\* (where type meets the requirement described in [Maximize Utilization](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#maximize-utilization)):

BaseAddress + width \* ty + tx

For these accesses to be fully coalesced, both the width of the thread block and the width of the array must be a multiple of the warp size.

In particular, this means that an array whose width is not a multiple of this size will be accessed much more efficiently if it is actually allocated with a width rounded up to the closest multiple of this size and its rows padded accordingly. The cudaMallocPitch() and cuMemAllocPitch() functions and associated memory copy functions described in the reference manual enable programmers to write non-hardware-dependent code to allocate arrays that conform to these constraints.

#### Local Memory

Local memory accesses only occur for some automatic variables as mentioned in [Variable Type Qualifiers](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#variable-type-qualifiers). Automatic variables that the compiler is likely to place in local memory are:

* Arrays for which it cannot determine that they are indexed with constant quantities,
* Large structures or arrays that would consume too much register space,
* Any variable if the kernel uses more registers than available (this is also known as register spilling).

Inspection of the PTX assembly code (obtained by compiling with the -ptx or-keep option) will tell if a variable has been placed in local memory during the first compilation phases as it will be declared using the .local mnemonic and accessed using the ld.local and st.local mnemonics. Even if it has not, subsequent compilation phases might still decide otherwise though if they find it consumes too much register space for the targeted architecture: Inspection of the cubin object using cuobjdump will tell if this is the case. Also, the compiler reports total local memory usage per kernel (lmem) when compiling with the --ptxas-options=-v option. Note that some mathematical functions have implementation paths that might access local memory.

The local memory space resides in device memory, so local memory accesses have same high latency and low bandwidth as global memory accesses and are subject to the same requirements for memory coalescing as described in [Device Memory Accesses](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#device-memory-accesses). Local memory is however organized such that consecutive 32-bit words are accessed by consecutive thread IDs. Accesses are therefore fully coalesced as long as all threads in a warp access the same relative address (e.g., same index in an array variable, same member in a structure variable).

On devices of compute capability 2.x and 3.x, local memory accesses are always cached in L1 and L2 in the same way as global memory accesses (see [Compute Capability 2.x](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compute-capability-2-x) and [Compute Capability 3.x](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compute-capability-3-0)).

On devices of compute capability 5.x, local memory accesses are always cached in L2 in the same way as global memory accesses (see [Compute Capability 5.x](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compute-capability-5-x)).

#### Shared Memory

Because it is on-chip, shared memory has much higher bandwidth and much lower latency than local or global memory.

To achieve high bandwidth, shared memory is divided into equally-sized memory modules, called banks, which can be accessed simultaneously. Any memory read or write request made of n addresses that fall in n distinct memory banks can therefore be serviced simultaneously, yielding an overall bandwidth that is n times as high as the bandwidth of a single module.

However, if two addresses of a memory request fall in the same memory bank, there is a bank conflict and the access has to be serialized. The hardware splits a memory request with bank conflicts into as many separate conflict-free requests as necessary, decreasing throughput by a factor equal to the number of separate memory requests. If the number of separate memory requests is n, the initial memory request is said to cause n-way bank conflicts.

To get maximum performance, it is therefore important to understand how memory addresses map to memory banks in order to schedule the memory requests so as to minimize bank conflicts. This is described in [Compute Capability 2.x](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compute-capability-2-x), [Compute Capability 3.x](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compute-capability-3-0), and [Compute Capability 5.x](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compute-capability-5-x) for devices of compute capability 2.x, 3.x, and 5.x, respectively.

#### Constant Memory

The constant memory space resides in device memory and is cached in the constant cache mentioned in [Compute Capability 2.x](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compute-capability-2-x).

A request is then split into as many separate requests as there are different memory addresses in the initial request, decreasing throughput by a factor equal to the number of separate requests.

The resulting requests are then serviced at the throughput of the constant cache in case of a cache hit, or at the throughput of device memory otherwise.

#### Texture and Surface Memory

The texture and surface memory spaces reside in device memory and are cached in texture cache, so a texture fetch or surface read costs one memory read from device memory only on a cache miss, otherwise it just costs one read from texture cache. The texture cache is optimized for 2D spatial locality, so threads of the same warp that read texture or surface addresses that are close together in 2D will achieve best performance. Also, it is designed for streaming fetches with a constant latency; a cache hit reduces DRAM bandwidth demand but not fetch latency.

Reading device memory through texture or surface fetching present some benefits that can make it an advantageous alternative to reading device memory from global or constant memory:

* If the memory reads do not follow the access patterns that global or constant memory reads must follow to get good performance, higher bandwidth can be achieved providing that there is locality in the texture fetches or surface reads;
* Addressing calculations are performed outside the kernel by dedicated units;
* Packed data may be broadcast to separate variables in a single operation;
* 8-bit and 16-bit integer input data may be optionally converted to 32 bit floating-point values in the range [0.0, 1.0] or [-1.0, 1.0] (see [Texture Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texture-memory)).

### [5.4. Maximize Instruction Throughput](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "maximize-instruction-throughput)

To maximize instruction throughput the application should:

* Minimize the use of arithmetic instructions with low throughput; this includes trading precision for speed when it does not affect the end result, such as using intrinsic instead of regular functions (intrinsic functions are listed in [Intrinsic Functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#intrinsic-functions)), single-precision instead of double-precision, or flushing denormalized numbers to zero;
* Minimize divergent warps caused by control flow instructions as detailed in [Control Flow Instructions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#control-flow-instructions)
* Reduce the number of instructions, for example, by optimizing out synchronization points whenever possible as described in [Synchronization Instruction](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#synchronization-instruction) or by using restricted pointers as described in [\_\_restrict\_\_](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#restrict).

In this section, throughputs are given in number of operations per clock cycle per multiprocessor. For a warp size of 32, one instruction corresponds to 32 operations, so if N is the number of operations per clock cycle, the instruction throughput is N/32 instructions per clock cycle.

All throughputs are for one multiprocessor. They must be multiplied by the number of multiprocessors in the device to get throughput for the whole device.

### [5.4.1. Arithmetic Instructions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "arithmetic-instructions)

[Table 2](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#arithmetic-instructions__throughput-native-arithmetic-instructions) gives the throughputs of the arithmetic instructions that are natively supported in hardware for devices of various compute capabilities.

| Table 2. Throughput of Native Arithmetic Instructions. (Number of Operations per Clock Cycle per Multiprocessor) | | | | | |
| --- | --- | --- | --- | --- | --- |
|  | **Compute Capability** | | | | |
| **2.0** | **2.1** | **3.0, 3.2** | **3.5, 3.7** | **5.x** |
| 32-bit floating-point add, multiply, multiply-add | 32 | 48 | 192 | 192 | 128 |
| 64-bit floating-point add, multiply, multiply-add | 16[1](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "fntarg_1) | 4 | 8 | 64[2](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "fntarg_2) | 1 |
| 32-bit floating-point reciprocal, reciprocal square root, base-2 logarithm (\_\_log2f), base 2 exponential (exp2f), sine (\_\_sinf), cosine (\_\_cosf) | 4 | 8 | 32 | 32 | 32 |
| 32-bit integer add, extended-precision add, subtract, extended-precision subtract | 32 | 48 | 160 | 160 | 128 |
| 32-bit integer multiply, multiply-add, extended-precision multiply-add | 16 | 16 | 32 | 32 | Multiple instructions |
| 24-bit integer multiply (\_\_[u]mul24) | Multiple instructions | Multiple instructions | Multiple instructions | Multiple instructions | Multiple instructions |
| 32-bit integer shift | 16 | 16 | 32 | 64[3](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "fntarg_3) | 64 |
| compare, minimum, maximum | 32 | 48 | 160 | 160 | 64 |
| 32-bit integer bit reverse, bit field extract/insert | 16 | 16 | 32 | 32 | 64 |
| 32-bit bitwise AND, OR, XOR | 32 | 48 | 160 | 160 | 128 |
| count of leading zeros, most significant non-sign bit | 16 | 16 | 32 | 32 | Multiple instructions |
| population count | 16 | 16 | 32 | 32 | 32 |
| warp shuffle | N/A | N/A | 32 | 32 | 32 |
| sum of absolute difference | 16 | 16 | 32 | 32 | 64 |
| SIMD video instructions vabsdiff2 | N/A | N/A | 160 | 160 | Multiple instructions |
| SIMD video instructions vabsdiff4 | N/A | N/A | 160 | 160 | Multiple instructions |
| All other SIMD video instructions | 16 | 16 | 32 | 32 | Multiple instructions |
| Type conversions from 8-bit and 16-bit integer to 32-bit types | 16 | 16 | 128 | 128 | 32 |
| Type conversions from and to 64-bit types | 16[4](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "fntarg_4) | 4 | 8 | 32[5](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "fntarg_5) | 4 |
| All other type conversions | 16 | 16 | 32 | 32 | 32 |

Other instructions and functions are implemented on top of the native instructions. The implementation may be different for devices of different compute capabilities, and the number of native instructions after compilation may fluctuate with every compiler version. For complicated functions, there can be multiple code paths depending on input. cuobjdump can be used to inspect a particular implementation in a cubin object.

The implementation of some functions are readily available on the CUDA header files (math\_functions.h, device\_functions.h, ...).

In general, code compiled with -ftz=true (denormalized numbers are flushed to zero) tends to have higher performance than code compiled with -ftz=false. Similarly, code compiled with -prec div=false (less precise division) tends to have higher performance code than code compiled with -prec div=true, and code compiled with -prec-sqrt=false (less precise square root) tends to have higher performance than code compiled with -prec-sqrt=true. The nvcc user manual describes these compilation flags in more details.

#### Single-Precision Floating-Point Division

\_\_fdividef(x, y) (see [Intrinsic Functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#intrinsic-functions)) provides faster single-precision floating-point division than the division operator.

#### Single-Precision Floating-Point Reciprocal Square Root

To preserve IEEE-754 semantics the compiler can optimize 1.0/sqrtf() into rsqrtf() only when both reciprocal and square root are approximate, (i.e., with -prec-div=false and -prec-sqrt=false). It is therefore recommended to invoke rsqrtf() directly where desired.

#### Single-Precision Floating-Point Square Root

Single-precision floating-point square root is implemented as a reciprocal square root followed by a reciprocal instead of a reciprocal square root followed by a multiplication so that it gives correct results for 0 and infinity.

#### Sine and Cosine

sinf(x), cosf(x), tanf(x), sincosf(x), and corresponding double-precision instructions are much more expensive and even more so if the argument x is large in magnitude.

More precisely, the argument reduction code (see [Mathematical Functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#mathematical-functions) for implementation) comprises two code paths referred to as the fast path and the slow path, respectively.

The fast path is used for arguments sufficiently small in magnitude and essentially consists of a few multiply-add operations. The slow path is used for arguments large in magnitude and consists of lengthy computations required to achieve correct results over the entire argument range.

At present, the argument reduction code for the trigonometric functions selects the fast path for arguments whose magnitude is less than 105615.0f for the single-precision functions, and less than 2147483648.0 for the double-precision functions.

As the slow path requires more registers than the fast path, an attempt has been made to reduce register pressure in the slow path by storing some intermediate variables in local memory, which may affect performance because of local memory high latency and bandwidth (see [Device Memory Accesses](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#device-memory-accesses)). At present, 28 bytes of local memory are used by single-precision functions, and 44 bytes are used by double-precision functions. However, the exact amount is subject to change.

Due to the lengthy computations and use of local memory in the slow path, the throughput of these trigonometric functions is lower by one order of magnitude when the slow path reduction is required as opposed to the fast path reduction.

#### Integer Arithmetic

Integer division and modulo operation are costly as they compiler to up to 20 instructions. They can be replaced with bitwise operations in some cases: If n is a power of 2, (i/n) is equivalent to (i>>log2(n)) and (i%n) is equivalent to (i&(n-1)); the compiler will perform these conversions if n is literal.

\_\_brev and \_\_popc map to a single instruction and \_\_brevll and \_\_popcll to a few instructions.

\_\_[u]mul24 are legacy intrinsic functions that have no longer any reason to be used.

#### Type Conversion

Sometimes, the compiler must insert conversion instructions, introducing additional execution cycles. This is the case for:

* Functions operating on variables of type char or short whose operands generally need to be converted to int,
* Double-precision floating-point constants (i.e., those constants defined without any type suffix) used as input to single-precision floating-point computations (as mandated by C/C++ standards).

This last case can be avoided by using single-precision floating-point constants, defined with an f suffix such as 3.141592653589793f, 1.0f, 0.5f.

### [5.4.2. Control Flow Instructions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "control-flow-instructions)

Any flow control instruction (if, switch, do, for, while) can significantly impact the effective instruction throughput by causing threads of the same warp to diverge (i.e., to follow different execution paths). If this happens, the different executions paths have to be serialized, increasing the total number of instructions executed for this warp. When all the different execution paths have completed, the threads converge back to the same execution path.

To obtain best performance in cases where the control flow depends on the thread ID, the controlling condition should be written so as to minimize the number of divergent warps. This is possible because the distribution of the warps across the block is deterministic as mentioned in [SIMT Architecture](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#simt-architecture). A trivial example is when the controlling condition only depends on (threadIdx / warpSize) where warpSize is the warp size. In this case, no warp diverges since the controlling condition is perfectly aligned with the warps.

Sometimes, the compiler may unroll loops or it may optimize out if or switch statements by using branch predication instead, as detailed below. In these cases, no warp can ever diverge. The programmer can also control loop unrolling using the #pragma unroll directive (see [#pragma unroll](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#pragma-unroll)).

When using branch predication none of the instructions whose execution depends on the controlling condition gets skipped. Instead, each of them is associated with a per-thread condition code or predicate that is set to true or false based on the controlling condition and although each of these instructions gets scheduled for execution, only the instructions with a true predicate are actually executed. Instructions with a false predicate do not write results, and also do not evaluate addresses or read operands.

The compiler replaces a branch instruction with predicated instructions only if the number of instructions controlled by the branch condition is less or equal to a certain threshold: If the compiler determines that the condition is likely to produce many divergent warps, this threshold is 7, otherwise it is 4.

### [5.4.3. Synchronization Instruction](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "synchronization-instruction)

Throughput for \_\_syncthreads() is 16 operations per clock cycle for devices of compute capability 2.x and 128 operations per clock cycle for devices of compute capability 3.x.

Note that \_\_syncthreads() can impact performance by forcing the multiprocessor to idle as detailed in [Device Memory Accesses](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#device-memory-accesses).

## [A. CUDA-Enabled GPUs](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "cuda-enabled-gpus)

<http://developer.nvidia.com/cuda-gpus> lists all CUDA-enabled devices with their compute capability.

The compute capability, number of multiprocessors, clock frequency, total amount of device memory, and other properties can be queried using the runtime (see reference manual).

## [B. C Language Extensions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "c-language-extensions)

### [B.1. Function Type Qualifiers](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "function-type-qualifiers)

Function type qualifiers specify whether a function executes on the host or on the device and whether it is callable from the host or from the device.

### [B.1.1. \_\_device\_\_](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "device-function-qualifier)

The \_\_device\_\_ qualifier declares a function that is:

* Executed on the device,
* Callable from the device only.

### [B.1.2. \_\_global\_\_](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "global)

The \_\_global\_\_ qualifier declares a function as being a kernel. Such a function is:

* Executed on the device,
* Callable from the host,
* Callable from the device for devices of compute capability 3.x (see [CUDA Dynamic Parallelism](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#cuda-dynamic-parallelism) for more details).

\_\_global\_\_ functions must have void return type.

Any call to a \_\_global\_\_ function must specify its execution configuration as described in [Execution Configuration](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#execution-configuration).

A call to a \_\_global\_\_ function is asynchronous, meaning it returns before the device has completed its execution.

### [B.1.3. \_\_host\_\_](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "host)

The \_\_host\_\_ qualifier declares a function that is:

* Executed on the host,
* Callable from the host only.

It is equivalent to declare a function with only the \_\_host\_\_ qualifier or to declare it without any of the \_\_host\_\_, \_\_device\_\_, or \_\_global\_\_ qualifier; in either case the function is compiled for the host only.

The \_\_global\_\_ and \_\_host\_\_ qualifiers cannot be used together.

The \_\_device\_\_ and \_\_host\_\_ qualifiers can be used together however, in which case the function is compiled for both the host and the device. The \_\_CUDA\_ARCH\_\_ macro introduced in [Application Compatibility](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#application-compatibility) can be used to differentiate code paths between host and device:

\_\_host\_\_ \_\_device\_\_ func()

{

#if \_\_CUDA\_ARCH\_\_ >= 500

// Device code path for compute capability 5.x

#elif \_\_CUDA\_ARCH\_\_ >= 300

// Device code path for compute capability 3.x

#elif \_\_CUDA\_ARCH\_\_ >= 200

// Device code path for compute capability 2.x

#elif !defined(\_\_CUDA\_ARCH\_\_)

// Host code path

#endif

}

### [B.1.4. \_\_noinline\_\_ and \_\_forceinline\_\_](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "noinline-and-forceinline)

The compiler inlines any \_\_device\_\_ function when deemed appropriate.

The \_\_noinline\_\_ function qualifier can be used as a hint for the compiler not to inline the function if possible. The function body must still be in the same file where it is called.

The \_\_forceinline\_\_ function qualifier can be used to force the compiler to inline the function.

### [B.2. Variable Type Qualifiers](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "variable-type-qualifiers)

Variable type qualifiers specify the memory location on the device of a variable.

An automatic variable declared in device code without any of the \_\_device\_\_, \_\_shared\_\_ and \_\_constant\_\_ qualifiers described in this section generally resides in a register. However in some cases the compiler might choose to place it in local memory, which can have adverse performance consequences as detailed in [Device Memory Accesses](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#device-memory-accesses).

### [B.2.1. \_\_device\_\_](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "device-variable-qualifier)

The \_\_device\_\_ qualifier declares a variable that resides on the device.

At most one of the other type qualifiers defined in the next two sections may be used together with \_\_device\_\_ to further specify which memory space the variable belongs to. If none of them is present, the variable:

* Resides in global memory space.
* Has the lifetime of an application.
* Is accessible from all the threads within the grid and from the host through the runtime library (cudaGetSymbolAddress() / cudaGetSymbolSize() / cudaMemcpyToSymbol() / cudaMemcpyFromSymbol()).
* May be additionally qualified with the \_\_managed\_\_ qualifier. Such a variable can be directly referenced from host code, e.g., its address can be taken or it can read or written directly from a host function. As a convenience, \_\_managed\_\_ implies \_\_managed\_\_\_\_device\_\_ i.e., the \_\_device\_\_ qualifier is implicit when the \_\_managed\_\_ qualifier is specified.

### [B.2.2. \_\_constant\_\_](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "constant)

The \_\_constant\_\_ qualifier, optionally used together with \_\_device\_\_, declares a variable that:

* Resides in constant memory space,
* Has the lifetime of an application,
* Is accessible from all the threads within the grid and from the host through the runtime library (cudaGetSymbolAddress() / cudaGetSymbolSize() / cudaMemcpyToSymbol() / cudaMemcpyFromSymbol()).

### [B.2.3. \_\_shared\_\_](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "shared)

The \_\_shared\_\_ qualifier, optionally used together with \_\_device\_\_, declares a variable that:

* Resides in the shared memory space of a thread block,
* Has the lifetime of the block,
* Is only accessible from all the threads within the block.

When declaring a variable in shared memory as an external array such as

extern \_\_shared\_\_ float shared[];

the size of the array is determined at launch time (see [Execution Configuration](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#execution-configuration)). All variables declared in this fashion, start at the same address in memory, so that the layout of the variables in the array must be explicitly managed through offsets. For example, if one wants the equivalent of

short array0[128];

float array1[64];

int array2[256];

in dynamically allocated shared memory, one could declare and initialize the arrays the following way:

extern \_\_shared\_\_ float array[];

\_\_device\_\_ void func() // \_\_device\_\_ or \_\_global\_\_ function

{

short\* array0 = (short\*)array;

float\* array1 = (float\*)&array0[128];

int\* array2 = (int\*)&array1[64];

}

Note that pointers need to be aligned to the type they point to, so the following code, for example, does not work since array1 is not aligned to 4 bytes.

extern \_\_shared\_\_ float array[];

\_\_device\_\_ void func() // \_\_device\_\_ or \_\_global\_\_ function

{

short\* array0 = (short\*)array;

float\* array1 = (float\*)&array0[127];

}

Alignment requirements for the built-in vector types are listed in [Table 3](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#vector-types__alignment-requirements-in-device-code).

### [B.2.4. \_\_restrict\_\_](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "restrict)

nvcc supports restricted pointers via the \_\_restrict\_\_ keyword.

Restricted pointers were introduced in C99 to alleviate the aliasing problem that exists in C-type languages, and which inhibits all kind of optimization from code re-ordering to common sub-expression elimination.

Here is an example subject to the aliasing issue, where use of restricted pointer can help the compiler to reduce the number of instructions:

void foo(const float\* a,

const float\* b,

float\* c)

{

c[0] = a[0] \* b[0];

c[1] = a[0] \* b[0];

c[2] = a[0] \* b[0] \* a[1];

c[3] = a[0] \* a[1];

c[4] = a[0] \* b[0];

c[5] = b[0];

...

}

In C-type languages, the pointers a, b, and c may be aliased, so any write through c could modify elements of a or b. This means that to guarantee functional correctness, the compiler cannot load a[0] and b[0] into registers, multiply them, and store the result to both c[0] and c[1], because the results would differ from the abstract execution model if, say, a[0] is really the same location as c[0]. So the compiler cannot take advantage of the common sub-expression. Likewise, the compiler cannot just reorder the computation of c[4] into the proximity of the computation of c[0] and c[1] because the preceding write to c[3] could change the inputs to the computation of c[4].

By making a, b, and c restricted pointers, the programmer asserts to the compiler that the pointers are in fact not aliased, which in this case means writes through c would never overwrite elements of a or b. This changes the function prototype as follows:

void foo(const float\* \_\_restrict\_\_ a,

const float\* \_\_restrict\_\_ b,

float\* \_\_restrict\_\_ c);

Note that all pointer arguments need to be made restricted for the compiler optimizer to derive any benefit. With the \_\_restrict\_\_ keywords added, the compiler can now reorder and do common sub-expression elimination at will, while retaining functionality identical with the abstract execution model:

void foo(const float\* \_\_restrict\_\_ a,

const float\* \_\_restrict\_\_ b,

float\* \_\_restrict\_\_ c)

{

float t0 = a[0];

float t1 = b[0];

float t2 = t0 \* t2;

float t3 = a[1];

c[0] = t2;

c[1] = t2;

c[4] = t2;

c[2] = t2 \* t3;

c[3] = t0 \* t3;

c[5] = t1;

...

}

The effects here are a reduced number of memory accesses and reduced number of computations. This is balanced by an increase in register pressure due to "cached" loads and common sub-expressions.

Since register pressure is a critical issue in many CUDA codes, use of restricted pointers can have negative performance impact on CUDA code, due to reduced occupancy.

### [B.3. Built-in Vector Types](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "built-in-vector-types)

### [B.3.1. char, short, int, long, longlong, float, double](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "vector-types)

These are vector types derived from the basic integer and floating-point types. They are structures and the 1st, 2nd, 3rd, and 4th components are accessible through the fields x, y, z, and w, respectively. They all come with a constructor function of the form make\_<type name>; for example,

int2 make\_int2(int x, int y);

which creates a vector of type int2 with value(x, y).

In host code, the alignment requirement of a vector type is equal to the alignment requirement of its base type. This is not always the case in device code as detailed in [Table 3](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#vector-types__alignment-requirements-in-device-code).

| Table 3. Alignment Requirements in Device Code | |
| --- | --- |
| **Type** | **Alignment** |
| char1, uchar1 | 1 |
| char2, uchar2 | 2 |
| char3, uchar3 | 1 |
| char4, uchar4 | 4 |
| short1, ushort1 | 2 |
| short2, ushort2 | 4 |
| short3, ushort3 | 2 |
| short4, ushort4 | 8 |
| int1, uint1 | 4 |
| int2, uint2 | 8 |
| int3, uint3 | 4 |
| int4, uint4 | 16 |
| long1, ulong1 | 4 if sizeof(long) is equal to sizeof(int) 8, otherwise |
| long2, ulong2 | 8 if sizeof(long) is equal to sizeof(int), 16, otherwise |
| long3, ulong3 | 4 if sizeof(long) is equal to sizeof(int), 8, otherwise |
| long4, ulong4 | 16 |
| longlong1, ulonglong1 | 8 |
| longlong2, ulonglong2 | 16 |
| float1 | 4 |
| float2 | 8 |
| float3 | 4 |
| float4 | 16 |
| double1 | 8 |
| double2 | 16 |

### [B.3.2. dim3](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "dim3)

This type is an integer vector type based on uint3 that is used to specify dimensions. When defining a variable of type dim3, any component left unspecified is initialized to 1.

### [B.4. Built-in Variables](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "built-in-variables)

Built-in variables specify the grid and block dimensions and the block and thread indices. They are only valid within functions that are executed on the device.

### [B.4.1. gridDim](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "griddim)

This variable is of type dim3 (see [dim3](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#dim3)) and contains the dimensions of the grid.

### [B.4.2. blockIdx](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "blockidx)

This variable is of type uint3 (see [char, short, int, long, longlong, float, double](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#vector-types)) and contains the block index within the grid.

### [B.4.3. blockDim](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "blockdim)

This variable is of type dim3 (see [dim3](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#dim3)) and contains the dimensions of the block.

### [B.4.4. threadIdx](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "threadidx)

This variable is of type uint3 (see [char, short, int, long, longlong, float, double](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#vector-types) ) and contains the thread index within the block.

### [B.4.5. warpSize](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "warpsize)

This variable is of type int and contains the warp size in threads (see [SIMT Architecture](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#simt-architecture) for the definition of a warp).

### [B.5. Memory Fence Functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "memory-fence-functions)

The CUDA programming model assumes a device with a weakly-ordered memory model, that is:

* The order in which a CUDA thread writes data to shared memory, global memory, page-locked host memory, or the memory of a peer device is not necessarily the order in which the data is observed being written by another CUDA or host thread;
* The order in which a CUDA thread reads data from shared memory, global memory, page-locked host memory, or the memory of a peer device is not necessarily the order in which the read instructions appear in the program for instructions that are independent of each other.

For example, if thread 0 executes writeXY() and thread 1 executes readXY() as defined in the following code sample

\_\_device\_\_ int X = 1, Y = 2;

\_\_device\_\_ void writeXY()

{

X = 10;

Y = 20;

}

\_\_device\_\_ void readXY()

{

int B = Y;

int A = X;

}

it is possible that A ends up equal to 1 and B equal to 20 for thread 1:

* either because at the time thread 1 reads X and Y, thread 0's write to Y has happened from thread 1's perspective, but thread 0's write to X has not,
* or because thread 1 reads Y before X and thread 0's writes to X and Y happen after thread 1's read of Y and before thread 1's read of X.

In a strongly-ordered memory model, the only possibilities would be:

* A equal to 1 and B equal to 2 (thread 0's writes to X and Y happen after thread 1's read of X and Y),
* A equal to 10 and B equal to 2 (thread 0's write to X happens before thread 1's read of X and thread 0's write to Y happens after thread 1's read of Y),
* A equal to 10 and B equal to 20 (thread 0's writes to X and Y happen before thread 1's read of X and Y),

Memory fence functions can be used to enforce some ordering:

void \_\_threadfence\_block();

ensures that:

* All writes to shared and global memory made by the calling thread before the call to \_\_threadfence\_block() are observed by all threads in the block of the calling thread as occurring before all writes to shared memory and global memory made by the calling thread after the call to \_\_threadfence\_block();
* All reads from shared memory and global memory made by the calling thread before the call to \_\_threadfence\_block() are performed before all reads from shared memory and global memory made by the calling thread after the call to \_\_threadfence\_block().

void \_\_threadfence();

acts as \_\_threadfence\_block() for all threads in the block of the calling thread and also ensures that all writes to global memory made by the calling thread before the call to \_\_threadfence() are observed by all threads in the device as occurring before all writes to global memory made by the calling thread after the call to \_\_threadfence().

void \_\_threadfence\_system();

acts as \_\_threadfence\_block() for all threads in the block of the calling thread and also ensures that:

* All writes to global memory, page-locked host memory, and the memory of a peer device made by the calling thread before the call to \_\_threadfence\_system() are observed by all threads in the device, host threads, and all threads in peer devices as occurring before all writes to global memory, page-locked host memory, and the memory of a peer device made by the calling thread after the call to \_\_threadfence\_system().
* All reads from shared memory, global memory, page-locked host memory, and the memory of a peer device made by the calling thread before the call to \_\_threadfence\_system() are performed before all reads from shared memory, global memory, page-locked host memory, and the memory of a peer device made by the calling thread after the call to \_\_threadfence\_system().

\_\_threadfence\_system() is only supported by devices of compute capability 2.x and higher.

In the previous code sample, inserting a fence function call between X = 10; and Y = 20; and between int A = X; and int B = Y; would ensure that for thread 1, A will always be equal to 10 if B is equal to 20. If thread 0 and 1 belong to the same block, it is enough to use \_\_threadfence\_block(). If thread 0 and 1 do not belong to the same block, \_\_threadfence() must be used if they are CUDA threads from the same device and \_\_threadfence\_system() must be used if they are CUDA threads from two different devices.

A common use case is when threads consume some data produced by other threads as illustrated by the following code sample of a kernel that computes the sum of an array of N numbers in one call. Each block first sums a subset of the array and stores the result in global memory. When all blocks are done, the last block done reads each of these partial sums from global memory and sums them to obtain the final result. In order to determine which block is finished last, each block atomically increments a counter to signal that it is done with computing and storing its partial sum (see [Atomic Functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#atomic-functions) about atomic functions). The last block is the one that receives the counter value equal to gridDim.x-1. If no fence is placed between storing the partial sum and incrementing the counter, the counter might increment before the partial sum is stored and therefore, might reach gridDim.x-1 and let the last block start reading partial sums before they have been actually updated in memory.

Memory fence functions only affect the ordering of memory operations by a thread; they do not ensure that these memory operations are visible to other threads (like \_\_syncthreads() does for threads within a block (see [Synchronization Functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#synchronization-functions))). In the code sample below, the visibility of memory operations on the result variable is ensured by declaring it as volatile (see [Volatile Qualifier](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#volatile-qualifier)).

\_\_device\_\_ unsigned int count = 0;

\_\_shared\_\_ bool isLastBlockDone;

\_\_global\_\_ void sum(const float\* array, unsigned int N,

volatile float\* result)

{

// Each block sums a subset of the input array.

float partialSum = calculatePartialSum(array, N);

if (threadIdx.x == 0) {

// Thread 0 of each block stores the partial sum

// to global memory. The compiler will use

// a store operation that bypasses the L1 cache

// since the "result" variable is declared as

// volatile. This ensures that the threads of

// the last block will read the correct partial

// sums computed by all other blocks.

result[blockIdx.x] = partialSum;

// Thread 0 makes sure that the incrementation

// of the "count" variable is only performed after

// the partial sum has been written to global memory.

\_\_threadfence();

// Thread 0 signals that it is done.

unsigned int value = atomicInc(&count, gridDim.x);

// Thread 0 determines if its block is the last

// block to be done.

isLastBlockDone = (value == (gridDim.x - 1));

}

// Synchronize to make sure that each thread reads

// the correct value of isLastBlockDone.

\_\_syncthreads();

if (isLastBlockDone) {

// The last block sums the partial sums

// stored in result[0 .. gridDim.x-1]

float totalSum = calculateTotalSum(result);

if (threadIdx.x == 0) {

// Thread 0 of last block stores the total sum

// to global memory and resets the count

// varialble, so that the next kernel call

// works properly.

result[0] = totalSum;

count = 0;

}

}

}

### [B.6. Synchronization Functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "synchronization-functions)

void \_\_syncthreads();

waits until all threads in the thread block have reached this point and all global and shared memory accesses made by these threads prior to \_\_syncthreads() are visible to all threads in the block.

\_\_syncthreads() is used to coordinate communication between the threads of the same block. When some threads within a block access the same addresses in shared or global memory, there are potential read-after-write, write-after-read, or write-after-write hazards for some of these memory accesses. These data hazards can be avoided by synchronizing threads in-between these accesses.

\_\_syncthreads() is allowed in conditional code but only if the conditional evaluates identically across the entire thread block, otherwise the code execution is likely to hang or produce unintended side effects.

Devices of compute capability 2.x and higher support three variations of \_\_syncthreads() described below.

int \_\_syncthreads\_count(int predicate);

is identical to \_\_syncthreads() with the additional feature that it evaluates predicate for all threads of the block and returns the number of threads for which predicate evaluates to non-zero.

int \_\_syncthreads\_and(int predicate);

is identical to \_\_syncthreads() with the additional feature that it evaluates predicate for all threads of the block and returns non-zero if and only if predicate evaluates to non-zero for all of them.

int \_\_syncthreads\_or(int predicate);

is identical to \_\_syncthreads() with the additional feature that it evaluates predicate for all threads of the block and returns non-zero if and only if predicate evaluates to non-zero for any of them.

### [B.7. Mathematical Functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "mathematical-functions)

The reference manual lists all C/C++ standard library mathematical functions that are supported in device code and all intrinsic functions that are only supported in device code.

[Mathematical Functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#mathematical-functions-appendix) provides accuracy information for some of these functions when relevant.

### [B.8. Texture Functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "texture-functions)

Texture objects are described in [Texture Object API](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texture-object-api)

Texture references are described in [Texture Reference API](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texture-reference-api)

Texture fetching is described in [Texture Fetching](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texture-fetching).

### [B.8.1. Texture Object API](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "texture-object-api-appendix)

### [B.8.1.1. tex1Dfetch()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "tex1dfetch-object)

template<class T>

T tex1Dfetch(cudaTextureObject\_t texObj, int x);

fetches the region of linear memory specified by the one-dimensional texture object texObj using integer texture coordinate x. tex1Dfetch() only works with non-normalized coordinates, so only the border and clamp addressing modes are supported. It does not perform any texture filtering. For integer types, it may optionally promote the integer to single-precision floating point.

### [B.8.1.2. tex1D()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "tex1d-object)

template<class T>

T tex1D(cudaTextureObject\_t texObj, float x);

template<class T>

T tex1D(cudaTextureObject\_t texObj, float x);

fetches the CUDA array specified by the one-dimensional texture object texObj using texture coordinate x.

### [B.8.1.3. tex2D()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "tex2d-object)

template<class T>

T tex2D(cudaTextureObject\_t texObj, float x, float y);

fetches the CUDA array or the region of linear memory specified by the two-dimensional texture object texObj using texture coordinates x and y.

### [B.8.1.4. tex3D()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "tex3d-object)

template<class T>

T tex3D(cudaTextureObject\_t texObj, float x, float y, float z);

fetches the CUDA array specified by the three-dimensional texture object texObj using texture coordinates x, y, and z.

### [B.8.1.5. tex1DLayered()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "tex1dlayered-object)

template<class T>

T tex1DLayered(cudaTextureObject\_t texObj, float x, int layer);

fetches the CUDA array specified by the one-dimensional texture object texObj using texture coordinate x and index layer, as described in [Layered Textures](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#layered-textures)

### [B.8.1.6. tex2DLayered()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "tex2dlayered-object)

template<class T>

T tex2DLayered(cudaTextureObject\_t texObj,

float x, float y, int layer);

fetches the CUDA array specified by the two-dimensional texture object texObj using texture coordinates x and y, and index layer, as described in [Layered Textures](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#layered-textures).

### [B.8.1.7. texCubemap()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "texcubemap-object)

template<class T>

T texCubemap(cudaTextureObject\_t texObj, float x, float y, float z);

fetches the CUDA array specified by the three-dimensional texture object texObj using texture coordinates x, y, and z, as described in Section [Cubemap Textures](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#cubemap-textures).

### [B.8.1.8. texCubemapLayered()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "texcubemaplayered-object)

template<class T>

T texCubemapLayered(cudaTextureObject\_t texObj,

float x, float y, float z, int layer);

fetches the CUDA array specified by the cubemap layered texture object texObj using texture coordinates x, y, and z, and index layer, as described in [Cubemap Layered Textures](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#cubemap-layered-textures).

### [B.8.1.9. tex2Dgather()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "tex2dgather-object)

template<class T>

T tex2Dgather(cudaTextureObject\_t texObj,

float x, float y, int comp = 0);

fetches the CUDA array specified by the 2D texture object texObj using texture coordinates x and y and the comp parameter as described in [Texture Gather](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texture-gather).

### [B.8.2. Texture Reference API](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "texture-reference-api-appendix)

### [B.8.2.1. tex1Dfetch()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "tex1dfetch)

template<class DataType>

Type tex1Dfetch(

texture<DataType, cudaTextureType1D,

cudaReadModeElementType> texRef,

int x);

float tex1Dfetch(

texture<unsigned char, cudaTextureType1D,

cudaReadModeNormalizedFloat> texRef,

int x);

float tex1Dfetch(

texture<signed char, cudaTextureType1D,

cudaReadModeNormalizedFloat> texRef,

int x);

float tex1Dfetch(

texture<unsigned short, cudaTextureType1D,

cudaReadModeNormalizedFloat> texRef,

int x);

float tex1Dfetch(

texture<signed short, cudaTextureType1D,

cudaReadModeNormalizedFloat> texRef,

int x);

fetches the region of linear memory bound to the one-dimensional texture reference texRef using integer texture coordinate x. tex1Dfetch() only works with non-normalized coordinates, so only the border and clamp addressing modes are supported. It does not perform any texture filtering. For integer types, it may optionally promote the integer to single-precision floating point.

Besides the functions shown above, 2-, and 4-tuples are supported; for example:

float4 tex1Dfetch(

texture<uchar4, cudaTextureType1D,

cudaReadModeNormalizedFloat> texRef,

int x);

fetches the region of linear memory bound to texture reference texRef using texture coordinate x.

### [B.8.2.2. tex1D()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "tex1d)

template<class DataType, enum cudaTextureReadMode readMode>

Type tex1D(texture<DataType, cudaTextureType1D, readMode> texRef,

float x);

fetches the CUDA array bound to the one-dimensional texture reference texRef using texture coordinate x. Type is equal to DataType except when readMode is equal to cudaReadModeNormalizedFloat (see [Texture Reference API](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texture-reference-api)), in which case Type is equal to the matching floating-point type.

### [B.8.2.3. tex2D()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "tex2d)

template<class DataType, enum cudaTextureReadMode readMode>

Type tex2D(texture<DataType, cudaTextureType2D, readMode> texRef,

float x, float y);

fetches the CUDA array or the region of linear memory bound to the two-dimensional texture reference texRef using texture coordinates x and y. Type is equal to DataType except when readMode is equal to cudaReadModeNormalizedFloat (see [Texture Reference API](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texture-reference-api)), in which case Type is equal to the matching floating-point type.

### [B.8.2.4. tex3D()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "tex3d)

template<class DataType, enum cudaTextureReadMode readMode>

Type tex3D(texture<DataType, cudaTextureType3D, readMode> texRef,

float x, float y, float z);

fetches the CUDA array bound to the three-dimensional texture reference texRef using texture coordinates x, y, and z. Type is equal to DataType except when readMode is equal to cudaReadModeNormalizedFloat (see [Texture Reference API](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texture-reference-api)), in which case Type is equal to the matching floating-point type.

### [B.8.2.5. tex1DLayered()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "tex1dlayered)

template<class DataType, enum cudaTextureReadMode readMode>

Type tex1DLayered(

texture<DataType, cudaTextureType1DLayered, readMode> texRef,

float x, int layer);

fetches the CUDA array bound to the one-dimensional layered texture reference texRef using texture coordinate x and index layer, as described in [Layered Textures](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#layered-textures). Type is equal to DataType except when readMode is equal to cudaReadModeNormalizedFloat (see [Texture Reference API](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texture-reference-api)), in which case Type is equal to the matching floating-point type.

### [B.8.2.6. tex2DLayered()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "tex2dlayered)

template<class DataType, enum cudaTextureReadMode readMode>

Type tex2DLayered(

texture<DataType, cudaTextureType2DLayered, readMode> texRef,

float x, float y, int layer);

fetches the CUDA array bound to the two-dimensional layered texture reference texRef using texture coordinates x and y, and index layer, as described in [Texture Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texture-memory). Type is equal to DataType except when readMode is equal to cudaReadModeNormalizedFloat (see [Texture Reference API](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texture-reference-api)), in which case Type is equal to the matching floating-point type.

### [B.8.2.7. texCubemap()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "texcubemap)

template<class DataType, enum cudaTextureReadMode readMode>

Type texCubemap(

texture<DataType, cudaTextureTypeCubemap, readMode> texRef,

float x, float y, float z);

fetches the CUDA array bound to the cubemap texture reference texRef using texture coordinates x, y, and z, as described in [Cubemap Textures](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#cubemap-textures). Type is equal to DataType except when readMode is equal to cudaReadModeNormalizedFloat (see [Texture Reference API](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texture-reference-api)), in which case Type is equal to the matching floating-point type.

### [B.8.2.8. texCubemapLayered()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "texcubemaplayered)

template<class DataType, enum cudaTextureReadMode readMode>

Type texCubemapLayered(

texture<DataType, cudaTextureTypeCubemapLayered, readMode> texRef,

float x, float y, float z, int layer);

fetches the CUDA array bound to the cubemap layered texture reference texRef using texture coordinates x, y, and z, and index layer, as described in [Cubemap Layered Textures](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#cubemap-layered-textures). Type is equal to DataType except when readMode is equal to cudaReadModeNormalizedFloat (see [Texture Reference API](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texture-reference-api)), in which case Type is equal to the matching floating-point type.

### [B.8.2.9. tex2Dgather()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "tex2dgather)

template<class DataType, enum cudaTextureReadMode readMode>

Type tex2Dgather(

texture<DataType, cudaTextureType2D, readMode> texRef,

float x, float y, int comp = 0);

fetches the CUDA array bound to the 2D texture reference texRef using texture coordinates x and y and the comp parameter as described in [Texture Gather](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texture-gather). Type is a 4-component vector type. It is based on the base type of DataType except when readMode is equal to cudaReadModeNormalizedFloat (see [Texture Reference API](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texture-reference-api)), in which case it is always float4.

### [B.9. Surface Functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "surface-functions)

Surface functions are only supported by devices of compute capability 2.0 and higher.

Surface objects are described in described in [Surface Object API](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#surface-object-api-appendix)

Surface references are described in [Surface Reference API](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#surface-reference-api-appendix).

In the sections below, boundaryMode specifies the boundary mode, that is how out-of-range surface coordinates are handled; it is equal to either cudaBoundaryModeClamp, in which case out-of-range coordinates are clamped to the valid range, or cudaBoundaryModeZero, in which case out-of-range reads return zero and out-of-range writes are ignored, or cudaBoundaryModeTrap, in which case out-of-range accesses cause the kernel execution to fail.

### [B.9.1. Surface Object API](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "surface-object-api-appendix)

### [B.9.1.1. surf1Dread()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "surf1dread-object)

template<class T>

T surf1Dread(cudaSurfaceObject\_t surfObj, int x,

boundaryMode = cudaBoundaryModeTrap);

reads the CUDA array specified by the one-dimensional surface object surfObj using coordinate x.

### [B.9.1.2. surf1Dwrite](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "surf1dwrite-object)

template<class T>

void surf1Dwrite(T data,

cudaSurfaceObject\_t surfObj,

int x,

boundaryMode = cudaBoundaryModeTrap);

writes value data to the CUDA array specified by the one-dimensional surface object surfObj at coordinate x.

### [B.9.1.3. surf2Dread()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "surf2dread-object)

template<class T>

T surf2Dread(cudaSurfaceObject\_t surfObj,

int x, int y,

boundaryMode = cudaBoundaryModeTrap);

template<class T>

void surf2Dread(T\* data,

cudaSurfaceObject\_t surfObj,

int x, int y,

boundaryMode = cudaBoundaryModeTrap);

reads the CUDA array specified by the two-dimensional surface object surfObj using coordinates x and y.

### [B.9.1.4. surf2Dwrite()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "surf2dwrite-object)

template<class T>

void surf2Dwrite(T data,

cudaSurfaceObject\_t surfObj,

int x, int y,

boundaryMode = cudaBoundaryModeTrap);

writes value data to the CUDA array specified by the two-dimensional surface object surfObj at coordinate x and y.

### [B.9.1.5. surf3Dread()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "surf3dread-object)

template<class T>

T surf3Dread(cudaSurfaceObject\_t surfObj,

int x, int y, int z,

boundaryMode = cudaBoundaryModeTrap);

template<class T>

void surf3Dread(T\* data,

cudaSurfaceObject\_t surfObj,

int x, int y, int z,

boundaryMode = cudaBoundaryModeTrap);

reads the CUDA array specified by the three-dimensional surface object surfObj using coordinates x, y, and z.

### [B.9.1.6. surf3Dwrite()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "surf3dwrite-object)

template<class T>

void surf3Dwrite(T data,

cudaSurfaceObject\_t surfObj,

int x, int y, int z,

boundaryMode = cudaBoundaryModeTrap);

writes value data to the CUDA array specified by the three-dimensional object surfObj at coordinate x, y, and z.

### [B.9.1.7. surf1DLayeredread()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "surf1dlayeredread-object)

template<class T>

T surf1DLayeredread(

cudaSurfaceObject\_t surfObj,

int x, int layer,

boundaryMode = cudaBoundaryModeTrap);

template<class T>

void surf1DLayeredread(T data,

cudaSurfaceObject\_t surfObj,

int x, int layer,

boundaryMode = cudaBoundaryModeTrap);

reads the CUDA array specified by the one-dimensional layered surface object surfObj using coordinate x and index layer.

### [B.9.1.8. surf1DLayeredwrite()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "surf1dlayeredwrite-object)

template<class Type>

void surf1DLayeredwrite(T data,

cudaSurfaceObject\_t surfObj,

int x, int layer,

boundaryMode = cudaBoundaryModeTrap);

writes value data to the CUDA array specified by the two-dimensional layered surface object surfObj at coordinate x and index layer.

### [B.9.1.9. surf2DLayeredread()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "surf2dlayeredread-object)

template<class T>

T surf2DLayeredread(

cudaSurfaceObject\_t surfObj,

int x, int y, int layer,

boundaryMode = cudaBoundaryModeTrap);

template<class T>

void surf2DLayeredread(T data,

cudaSurfaceObject\_t surfObj,

int x, int y, int layer,

boundaryMode = cudaBoundaryModeTrap);

reads the CUDA array specified by the two-dimensional layered surface object surfObj using coordinate x and y, and index layer.

### [B.9.1.10. surf2DLayeredwrite()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "surf2dlayeredwrite-object)

template<class T>

void surf2DLayeredwrite(T data,

cudaSurfaceObject\_t surfObj,

int x, int y, int layer,

boundaryMode = cudaBoundaryModeTrap);

writes value data to the CUDA array specified by the one-dimensional layered surface object surfObj at coordinate x and y, and index layer.

### [B.9.1.11. surfCubemapread()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "surfcubemapread-object)

template<class T>

T surfCubemapread(

cudaSurfaceObject\_t surfObj,

int x, int y, int face,

boundaryMode = cudaBoundaryModeTrap);

template<class T>

void surfCubemapread(T data,

cudaSurfaceObject\_t surfObj,

int x, int y, int face,

boundaryMode = cudaBoundaryModeTrap);

reads the CUDA array specified by the cubemap surface object surfObj using coordinate x and y, and face index face.

### [B.9.1.12. surfCubemapwrite()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "surfcubemapwrite-object)

template<class T>

void surfCubemapwrite(T data,

cudaSurfaceObject\_t surfObj,

int x, int y, int face,

boundaryMode = cudaBoundaryModeTrap);

writes value data to the CUDA array specified by the cubemap object surfObj at coordinate x and y, and face index face.

### [B.9.1.13. surfCubemapLayeredread()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "surfcubemaplayeredread-object)

template<class T>

T surfCubemapLayeredread(

cudaSurfaceObject\_t surfObj,

int x, int y, int layerFace,

boundaryMode = cudaBoundaryModeTrap);

template<class T>

void surfCubemapLayeredread(T data,

cudaSurfaceObject\_t surfObj,

int x, int y, int layerFace,

boundaryMode = cudaBoundaryModeTrap);

reads the CUDA array specified by the cubemap layered surface object surfObj using coordinate x and y, and index layerFace.

### [B.9.1.14. surfCubemapLayeredwrite()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "surfcubemaplayeredwrite-object)

template<class T>

void surfCubemapLayeredwrite(T data,

cudaSurfaceObject\_t surfObj,

int x, int y, int layerFace,

boundaryMode = cudaBoundaryModeTrap);

writes value data to the CUDA array specified by the cubemap layered object surfObj at coordinate x and y, and index layerFace.

### [B.9.2. Surface Reference API](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "surface-reference-api-appendix)

### [B.9.2.1. surf1Dread()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "surf1dread)

template<class Type>

Type surf1Dread(surface<void, cudaSurfaceType1D> surfRef,

int x,

boundaryMode = cudaBoundaryModeTrap);

template<class Type>

void surf1Dread(Type data,

surface<void, cudaSurfaceType1D> surfRef,

int x,

boundaryMode = cudaBoundaryModeTrap);

reads the CUDA array bound to the one-dimensional surface reference surfRef using coordinate x.

### [B.9.2.2. surf1Dwrite](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "surf1dwrite)

template<class Type>

void surf1Dwrite(Type data,

surface<void, cudaSurfaceType1D> surfRef,

int x,

boundaryMode = cudaBoundaryModeTrap);

writes value data to the CUDA array bound to the one-dimensional surface reference surfRef at coordinate x.

### [B.9.2.3. surf2Dread()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "surf2dread)

template<class Type>

Type surf2Dread(surface<void, cudaSurfaceType2D> surfRef,

int x, int y,

boundaryMode = cudaBoundaryModeTrap);

template<class Type>

void surf2Dread(Type\* data,

surface<void, cudaSurfaceType2D> surfRef,

int x, int y,

boundaryMode = cudaBoundaryModeTrap);

reads the CUDA array bound to the two-dimensional surface reference surfRef using coordinates x and y.

### [B.9.2.4. surf2Dwrite()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "surf2dwrite)

template<class Type>

void surf3Dwrite(Type data,

surface<void, cudaSurfaceType3D> surfRef,

int x, int y, int z,

boundaryMode = cudaBoundaryModeTrap);

writes value data to the CUDA array bound to the two-dimensional surface reference surfRef at coordinate x and y.

### [B.9.2.5. surf3Dread()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "surf3dread)

template<class Type>

Type surf3Dread(surface<void, cudaSurfaceType3D> surfRef,

int x, int y, int z,

boundaryMode = cudaBoundaryModeTrap);

template<class Type>

void surf3Dread(Type\* data,

surface<void, cudaSurfaceType3D> surfRef,

int x, int y, int z,

boundaryMode = cudaBoundaryModeTrap);

reads the CUDA array bound to the three-dimensional surface reference surfRef using coordinates x, y, and z.

### [B.9.2.6. surf3Dwrite()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "surf3dwrite)

template<class Type>

void surf3Dwrite(Type data,

surface<void, cudaSurfaceType3D> surfRef,

int x, int y, int z,

boundaryMode = cudaBoundaryModeTrap);

writes value data to the CUDA array bound to the three-dimensional surface reference surfRef at coordinate x, y, and z.

### [B.9.2.7. surf1DLayeredread()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "surf1dlayeredread)

template<class Type>

Type surf1DLayeredread(

surface<void, cudaSurfaceType1DLayered> surfRef,

int x, int layer,

boundaryMode = cudaBoundaryModeTrap);

template<class Type>

void surf1DLayeredread(Type data,

surface<void, cudaSurfaceType1DLayered> surfRef,

int x, int layer,

boundaryMode = cudaBoundaryModeTrap);

reads the CUDA array bound to the one-dimensional layered surface reference surfRef using coordinate x and index layer.

### [B.9.2.8. surf1DLayeredwrite()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "surf1dlayeredwrite)

template<class Type>

void surf1DLayeredwrite(Type data,

surface<void, cudaSurfaceType1DLayered> surfRef,

int x, int layer,

boundaryMode = cudaBoundaryModeTrap);

writes value data to the CUDA array bound to the two-dimensional layered surface reference surfRef at coordinate x and index layer.

### [B.9.2.9. surf2DLayeredread()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "surf2dlayeredread)

template<class Type>

Type surf2DLayeredread(

surface<void, cudaSurfaceType2DLayered> surfRef,

int x, int y, int layer,

boundaryMode = cudaBoundaryModeTrap);

template<class Type>

void surf2DLayeredread(Type data,

surface<void, cudaSurfaceType2DLayered> surfRef,

int x, int y, int layer,

boundaryMode = cudaBoundaryModeTrap);

reads the CUDA array bound to the two-dimensional layered surface reference surfRef using coordinate x and y, and index layer.

### [B.9.2.10. surf2DLayeredwrite()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "surf2dlayeredwrite)

template<class Type>

void surf2DLayeredwrite(Type data,

surface<void, cudaSurfaceType2DLayered> surfRef,

int x, int y, int layer,

boundaryMode = cudaBoundaryModeTrap);

writes value data to the CUDA array bound to the one-dimensional layered surface reference surfRef at coordinate x and y, and index layer.

### [B.9.2.11. surfCubemapread()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "surfcubemapread)

template<class Type>

Type surfCubemapread(

surface<void, cudaSurfaceTypeCubemap> surfRef,

int x, int y, int face,

boundaryMode = cudaBoundaryModeTrap);

template<class Type>

void surfCubemapread(Type data,

surface<void, cudaSurfaceTypeCubemap> surfRef,

int x, int y, int face,

boundaryMode = cudaBoundaryModeTrap);

reads the CUDA array bound to the cubemap surface reference surfRef using coordinate x and y, and face index face.

### [B.9.2.12. surfCubemapwrite()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "surfcubemapwrite)

template<class Type>

void surfCubemapwrite(Type data,

surface<void, cudaSurfaceTypeCubemap> surfRef,

int x, int y, int face,

boundaryMode = cudaBoundaryModeTrap);

writes value data to the CUDA array bound to the cubemap reference surfRef at coordinate x and y, and face index face.

### [B.9.2.13. surfCubemapLayeredread()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "surfcubemaplayeredread)

template<class Type>

Type surfCubemapLayeredread(

surface<void, cudaSurfaceTypeCubemapLayered> surfRef,

int x, int y, int layerFace,

boundaryMode = cudaBoundaryModeTrap);

template<class Type>

void surfCubemapLayeredread(Type data,

surface<void, cudaSurfaceTypeCubemapLayered> surfRef,

int x, int y, int layerFace,

boundaryMode = cudaBoundaryModeTrap);

reads the CUDA array bound to the cubemap layered surface reference surfRef using coordinate x and y, and index layerFace.

### [B.9.2.14. surfCubemapLayeredwrite()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "surfcubemaplayeredwrite)

template<class Type>

void surfCubemapLayeredwrite(Type data,

surface<void, cudaSurfaceTypeCubemapLayered> surfRef,

int x, int y, int layerFace,

boundaryMode = cudaBoundaryModeTrap);

writes value data to the CUDA array bound to the cubemap layered reference surfRef at coordinate x and y, and index layerFace.

### [B.10. Read-Only Data Cache Load Function](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "ldg-function)

The read-only data cache load function is only supported by devices of compute capability 3.5 and higher.

T \_\_ldg(const T\* address);

returns the data of type T located at address address, where T is char, short, int, long longunsigned char, unsigned short, unsigned int, unsigned long long, int2, int4, uint2, uint4, float, float2, float4, double, or double2. The operation is cached in the read-only data cache (see [Global Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#global-memory-3-0)).

### [B.11. Time Function](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "time-function)

clock\_t clock();

long long int clock64();

when executed in device code, returns the value of a per-multiprocessor counter that is incremented every clock cycle. Sampling this counter at the beginning and at the end of a kernel, taking the difference of the two samples, and recording the result per thread provides a measure for each thread of the number of clock cycles taken by the device to completely execute the thread, but not of the number of clock cycles the device actually spent executing thread instructions. The former number is greater than the latter since threads are time sliced.

### [B.12. Atomic Functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "atomic-functions)

An atomic function performs a read-modify-write atomic operation on one 32-bit or 64-bit word residing in global or shared memory. For example, atomicAdd() reads a word at some address in global or shared memory, adds a number to it, and writes the result back to the same address. The operation is atomic in the sense that it is guaranteed to be performed without interference from other threads. In other words, no other thread can access this address until the operation is complete. Atomic functions can only be used in device functions and atomic functions operating on mapped page-locked memory ([Mapped Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#mapped-memory)) are not atomic from the point of view of the host or other devices.

Note that any atomic operation can be implemented based on atomicCAS() (Compare And Swap). For example, atomicAdd() for double-precision floating-point numbers can be implemented as follows:

\_\_device\_\_ double atomicAdd(double\* address, double val)

{

unsigned long long int\* address\_as\_ull =

(unsigned long long int\*)address;

unsigned long long int old = \*address\_as\_ull, assumed;

do {

assumed = old;

old = atomicCAS(address\_as\_ull, assumed,

\_\_double\_as\_longlong(val +

\_\_longlong\_as\_double(assumed)));

// Note: uses integer comparison to avoid hang in case of NaN (since NaN != NaN)

} while (assumed != old);

return \_\_longlong\_as\_double(old);

}

### [B.12.1. Arithmetic Functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "arithmetic-functions)

### [B.12.1.1. atomicAdd()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "atomicadd)

int atomicAdd(int\* address, int val);

unsigned int atomicAdd(unsigned int\* address,

unsigned int val);

unsigned long long int atomicAdd(unsigned long long int\* address,

unsigned long long int val);

float atomicAdd(float\* address, float val);

reads the 32-bit or 64-bit word old located at the address address in global or shared memory, computes (old + val), and stores the result back to memory at the same address. These three operations are performed in one atomic transaction. The function returns old.

The floating-point version of atomicAdd() is only supported by devices of compute capability 2.x and higher.

### [B.12.1.2. atomicSub()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "atomicsub)

int atomicSub(int\* address, int val);

unsigned int atomicSub(unsigned int\* address,

unsigned int val);

reads the 32-bit word old located at the address address in global or shared memory, computes (old - val), and stores the result back to memory at the same address. These three operations are performed in one atomic transaction. The function returns old.

### [B.12.1.3. atomicExch()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "atomicexch)

int atomicExch(int\* address, int val);

unsigned int atomicExch(unsigned int\* address,

unsigned int val);

unsigned long long int atomicExch(unsigned long long int\* address,

unsigned long long int val);

float atomicExch(float\* address, float val);

reads the 32-bit or 64-bit word old located at the address address in global or shared memory and stores val back to memory at the same address. These two operations are performed in one atomic transaction. The function returns old.

### [B.12.1.4. atomicMin()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "atomicmin)

int atomicMin(int\* address, int val);

unsigned int atomicMin(unsigned int\* address,

unsigned int val);

unsigned long long int atomicMin(unsigned long long int\* address,

unsigned long long int val);

reads the 32-bit or 64-bit word old located at the address address in global or shared memory, computes the minimum of old and val, and stores the result back to memory at the same address. These three operations are performed in one atomic transaction. The function returns old.

The 64-bit version of atomicMin() is only supported by devices of compute capability 3.5 and higher.

### [B.12.1.5. atomicMax()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "atomicmax)

int atomicMax(int\* address, int val);

unsigned int atomicMax(unsigned int\* address,

unsigned int val);

unsigned long long int atomicMax(unsigned long long int\* address,

unsigned long long int val);

reads the 32-bit or 64-bit word old located at the address address in global or shared memory, computes the maximum of old and val, and stores the result back to memory at the same address. These three operations are performed in one atomic transaction. The function returns old.

The 64-bit version of atomicMax() is only supported by devices of compute capability 3.5 and higher.

### [B.12.1.6. atomicInc()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "atomicinc)

unsigned int atomicInc(unsigned int\* address,

unsigned int val);

reads the 32-bit word old located at the address address in global or shared memory, computes ((old >= val) ? 0 : (old+1)), and stores the result back to memory at the same address. These three operations are performed in one atomic transaction. The function returns old.

### [B.12.1.7. atomicDec()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "atomicdec)

unsigned int atomicDec(unsigned int\* address,

unsigned int val);

reads the 32-bit word old located at the address address in global or shared memory, computes (((old == 0) | (old > val)) ? val : (old-1) ), and stores the result back to memory at the same address. These three operations are performed in one atomic transaction. The function returns old.

### [B.12.1.8. atomicCAS()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "atomiccas)

int atomicCAS(int\* address, int compare, int val);

unsigned int atomicCAS(unsigned int\* address,

unsigned int compare,

unsigned int val);

unsigned long long int atomicCAS(unsigned long long int\* address,

unsigned long long int compare,

unsigned long long int val);

reads the 32-bit or 64-bit word old located at the address address in global or shared memory, computes (old == compare ? val : old) , and stores the result back to memory at the same address. These three operations are performed in one atomic transaction. The function returns old (Compare And Swap).

### [B.12.2. Bitwise Functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "bitwise-functions)

### [B.12.2.1. atomicAnd()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "atomicand)

int atomicAnd(int\* address, int val);

unsigned int atomicAnd(unsigned int\* address,

unsigned int val);

unsigned long long int atomicAnd(unsigned long long int\* address,

unsigned long long int val);

reads the 32-bit or 64-bit word old located at the address address in global or shared memory, computes (old & val), and stores the result back to memory at the same address. These three operations are performed in one atomic transaction. The function returns old.

The 64-bit version of atomicAnd() is only supported by devices of compute capability 3.5 and higher.

### [B.12.2.2. atomicOr()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "atomicor)

int atomicOr(int\* address, int val);

unsigned int atomicOr(unsigned int\* address,

unsigned int val);

unsigned long long int atomicOr(unsigned long long int\* address,

unsigned long long int val);

reads the 32-bit or 64-bit word old located at the address address in global or shared memory, computes (old | val), and stores the result back to memory at the same address. These three operations are performed in one atomic transaction. The function returns old.

The 64-bit version of atomicOr() is only supported by devices of compute capability 3.5 and higher.

### [B.12.2.3. atomicXor()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "atomicxor)

int atomicXor(int\* address, int val);

unsigned int atomicXor(unsigned int\* address,

unsigned int val);

unsigned long long int atomicXor(unsigned long long int\* address,

unsigned long long int val);

reads the 32-bit or 64-bit word old located at the address address in global or shared memory, computes (old ^ val), and stores the result back to memory at the same address. These three operations are performed in one atomic transaction. The function returns old.

The 64-bit version of atomicXor() is only supported by devices of compute capability 3.5 and higher.

### [B.13. Warp Vote Functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "warp-vote-functions)

int \_\_all(int predicate);

int \_\_any(int predicate);

unsigned int \_\_ballot(int predicate);

The warp vote functions allow the threads of a given [warp](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#simt-architecture) to perform a reduction-and-broadcast operation. These functions take as input an integer predicate from each thread in the warp and compare those values with zero. The results of the comparisons are combined (reduced) across the [active](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#simt-architecture__notes) threads of the warp in one of the following ways, broadcasting a single return value to each participating thread:

\_\_all(predicate):

Evaluate predicate for all active threads of the warp and return non-zero if and only if predicate evaluates to non-zero for all of them.

\_\_any(predicate):

Evaluate predicate for all active threads of the warp and return non-zero if and only if predicate evaluates to non-zero for any of them.

\_\_ballot(predicate):

Evaluate predicate for all active threads of the warp and return an integer whose Nth bit is set if and only if predicate evaluates to non-zero for the Nth thread of the warp and the Nth thread is active.

### Notes

For each of these warp vote operations, the result excludes threads that are [inactive](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#simt-architecture__notes) (e.g., due to warp divergence). Inactive threads are represented by 0 bits in the value returned by \_\_ballot() and are not considered in the reductions performed by \_\_all() and \_\_any().

### [B.14. Warp Shuffle Functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "warp-shuffle-functions)

\_\_shfl, \_\_shfl\_up, \_\_shfl\_down, \_\_shfl\_xor exchange a variable between threads within a [warp](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#simt-architecture).

Supported by devices of compute capability 3.x.

### [B.14.1. Synopsis](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "synopsis)

int \_\_shfl(int var, int srcLane, int width=warpSize);

int \_\_shfl\_up(int var, unsigned int delta, int width=warpSize);

int \_\_shfl\_down(int var, unsigned int delta, int width=warpSize);

int \_\_shfl\_xor(int var, int laneMask, int width=warpSize);

float \_\_shfl(float var, int srcLane, int width=warpSize);

float \_\_shfl\_up(float var, unsigned int delta,

int width=warpSize);

float \_\_shfl\_down(float var, unsigned int delta,

int width=warpSize);

float \_\_shfl\_xor(float var, int laneMask, int width=warpSize);

### [B.14.2. Description](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "warp-description)

The \_\_shfl() intrinsics permit exchanging of a variable between threads within a warp without use of shared memory. The exchange occurs simultaneously for all [active](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#simt-architecture__notes) threads within the warp, moving 4 bytes of data per thread. Exchange of 8-byte quantities must be broken into two separate invocations of \_\_shfl().

Threads within a warp are referred to as lanes, and for devices of compute capability 3.x may have an index between 0 and warpSize-1 (inclusive). Four source-lane addressing modes are supported:

\_\_shfl()

Direct copy from indexed lane

\_\_shfl\_up()

Copy from a lane with lower ID relative to caller

\_\_shfl\_down()

Copy from a lane with higher ID relative to caller

\_\_shfl\_xor()

Copy from a lane based on bitwise XOR of own lane ID

Threads may only read data from another thread which is actively participating in the \_\_shfl() command. If the target thread is [inactive](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#simt-architecture__notes), the retrieved value is undefined.

All the \_\_shfl() intrinsics take an optional width parameter which permits sub-division of the warp into segments - for example to exchange data between 4 groups of 8 lanes in a SIMD manner. If width is less than warpSize then each subsection of the warp behaves as a separate entity with a starting logical lane ID of 0. A thread may only exchange data with others in its own subsection. width must have a value which is a power of 2 so that the warp can be subdivided equally; results are undefined if width is not a power of 2, or is a number greater than warpSize.

\_\_shfl() returns the value of var held by the thread whose ID is given by srcLane. If srcLane is outside the range [0:width-1], then the thread's own value of var is returned.

\_\_shfl\_up() calculates a source lane ID by subtracting delta from the caller's lane ID. The value of var held by the resulting lane ID is returned: in effect, var is shifted up the warp by delta lanes. The source lane index will not wrap around the value of width, so effectively the lower delta lanes will be unchanged.

\_\_shfl\_down() calculates a source lane ID by adding delta to the caller's lane ID. The value of var held by the resulting lane ID is returned: this has the effect of shifting var down the warp by delta lanes. As for \_\_shfl\_up(), the ID number of the source lane will not wrap around the value of width and so the upper delta lanes will remain unchanged.

\_\_shfl\_xor() calculates a source line ID by performing a bitwise XOR of the caller's lane ID with laneMask: the value of var held by the resulting lane ID is returned. If the resulting lane ID falls outside the range permitted by width, the thread's own value of var is returned. This mode implements a butterfly addressing pattern such as is used in tree reduction and broadcast.

### [B.14.3. Return Value](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "return-value)

All \_\_shfl() intrinsics return the 4-byte word referenced by var from the source lane ID as an unsigned integer. If the source lane ID is out of range or the source thread has exited, the calling thread's own var is returned.

### [B.14.4. Notes](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "warp-notes)

All \_\_shfl() intrinsics share the same semantics with respect to code motion as the vote intrinsics \_\_any() and \_\_all().

Threads may only read data from another thread which is actively participating in the \_\_shfl() command. If the target thread is inactive, the retrieved value is undefined.

width must be a power-of-2 (i.e., 2, 4, 8, 16 or 32). Results are unspecified for other values.

Types other than int or float must first be cast in order to use the \_\_shfl() intrinsics.

### [B.14.5. Examples](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "warp-examples)

### [B.14.5.1. Broadcast of a single value across a warp](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "warp-examples-broadcast)

#include <stdio.h>

\_\_global\_\_ void bcast(int arg) {

int laneId = threadIdx.x & 0x1f;

int value;

if (laneId == 0) // Note unused variable for

value = arg; // all threads except lane 0

value = \_\_shfl(value, 0); // Get "value" from lane 0

if (value != arg)

printf("Thread %d failed.\n", threadIdx.x);

}

int main() {

bcast<<< 1, 32 >>>(1234);

cudaDeviceSynchronize();

return 0;

}

### [B.14.5.2. Inclusive plus-scan across sub-partitions of 8 threads](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "warp-examples-inclusive)

#include <stdio.h>

\_\_global\_\_ void scan4() {

int laneId = threadIdx.x & 0x1f;

// Seed sample starting value (inverse of lane ID)

int value = 31 - laneId;

// Loop to accumulate scan within my partition.

// Scan requires log2(n) == 3 steps for 8 threads

// It works by an accumulated sum up the warp

// by 1, 2, 4, 8 etc. steps.

for (int i=1; i<=4; i\*=2) {

// Note: shfl requires all threads being

// accessed to be active. Therefore we do

// the \_\_shfl unconditionally so that we

// can read even from threads which won't do a

// sum, and then conditionally assign the result.

int n = \_\_shfl\_up(value, i, 8);

if (laneId >= i)

value += n;

}

printf("Thread %d final value = %d\n", threadIdx.x, value);

}

int main() {

scan4<<< 1, 32 >>>();

cudaDeviceSynchronize();

return 0;

}

### [B.14.5.3. Reduction across a warp](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "warp-examples-reduction)

#include <stdio.h>

\_\_global\_\_ void warpReduce() {

int laneId = threadIdx.x & 0x1f;

// Seed starting value as inverse lane ID

int value = 31 - laneId;

// Use XOR mode to perform butterfly reduction

for (int i=16; i>=1; i/=2)

value += \_\_shfl\_xor(value, i, 32);

// "value" now contains the sum across all threads

printf("Thread %d final value = %d\n", threadIdx.x, value);

}

int main() {

warpReduce<<< 1, 32 >>>();

cudaDeviceSynchronize();

return 0;

}

### [B.15. Profiler Counter Function](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "profiler-counter-function)

Each multiprocessor has a set of sixteen hardware counters that an application can increment with a single instruction by calling the \_\_prof\_trigger() function.

[void \_\_prof\_trigger(int counter);

increments by one per warp the per-multiprocessor hardware counter of index counter. Counters 8 to 15 are reserved and should not be used by applications.

The value of counters 0, 1, ..., 7 can be obtained via nvprof by nvprof --events prof\_trigger\_0x where x is 0, 1, ..., 7. The value of those counters for the first multiprocessor can also be obtained via the old CUDA command-line profiler by listing prof\_trigger\_00, prof\_trigger\_01, ..., prof\_trigger\_07 , etc. in the profiler.conf file (see the profiler manual for more details). All counters are reset before each kernel launch (note that when collecting counters, kernel launches are synchronous as mentioned in [Concurrent Execution between Host and Device](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#concurrent-execution-host-device)).

### [B.16. Assertion](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "assertion)

Assertion is only supported by devices of compute capability 2.x and higher. It is not supported on MacOS, regardless of the device, and loading a module that references the assert function on Mac OS will fail.

void assert(int expression);

stops the kernel execution if expression is equal to zero. If the program is run within a debugger, this triggers a breakpoint and the debugger can be used to inspect the current state of the device. Otherwise, each thread for which expression is equal to zero prints a message to stderr after synchronization with the host via cudaDeviceSynchronize(), cudaStreamSynchronize(), or cudaEventSynchronize(). The format of this message is as follows:

<filename>:<line number>:<function>:

block: [blockId.x,blockId.x,blockIdx.z],

thread: [threadIdx.x,threadIdx.y,threadIdx.z]

Assertion `<expression>` failed.

Any subsequent host-side synchronization calls made for the same device will return cudaErrorAssert. No more commands can be sent to this device until cudaDeviceReset() is called to reinitialize the device.

If expression is different from zero, the kernel execution is unaffected.

For example, the following program from source file test.cu

#include <assert.h>

\_\_global\_\_ void testAssert(void)

{

int is\_one = 1;

int should\_be\_one = 0;

// This will have no effect

assert(is\_one);

// This will halt kernel execution

assert(should\_be\_one);

}

int main(int argc, char\* argv[])

{

testAssert<<<1,1>>>();

cudaDeviceSynchronize();

return 0;

}

will output:

test.cu:19: void testAssert(): block: [0,0,0], thread: [0,0,0] Assertion `should\_be\_one` failed.

Assertions are for debugging purposes. They can affect performance and it is therefore recommended to disable them in production code. They can be disabled at compile time by defining the NDEBUG preprocessor macro before including assert.h. Note that expression should not be an expression with side effects (something like (++i > 0), for example), otherwise disabling the assertion will affect the functionality of the code.

### [B.17. Formatted Output](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "formatted-output)

Formatted output is only supported by devices of compute capability 2.x and higher.

int printf(const char \*format[, arg, ...]);

prints formatted output from a kernel to a host-side output stream.

The in-kernel printf() function behaves in a similar way to the standard C-library printf() function, and the user is referred to the host system's manual pages for a complete description of printf() behavior. In essence, the string passed in as format is output to a stream on the host, with substitutions made from the argument list wherever a format specifier is encountered. Supported format specifiers are listed below.

The printf() command is executed as any other device-side function: per-thread, and in the context of the calling thread. From a multi-threaded kernel, this means that a straightforward call to printf() will be executed by every thread, using that thread's data as specified. Multiple versions of the output string will then appear at the host stream, once for each thread which encountered the printf().

It is up to the programmer to limit the output to a single thread if only a single output string is desired (see [Examples](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#examples-per-thread) for an illustrative example).

Unlike the C-standard printf(), which returns the number of characters printed, CUDA's printf() returns the number of arguments parsed. If no arguments follow the format string, 0 is returned. If the format string is NULL, -1 is returned. If an internal error occurs, -2 is returned.

### [B.17.1. Format Specifiers](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "format-specifiers)

As for standard printf(), format specifiers take the form: %[flags][width][.precision][size]type

The following fields are supported (see widely-available documentation for a complete description of all behaviors):

* Flags: `#' ` ' `0' `+' `-'
* Width: `\*' `0-9'
* Precision: `0-9'
* Size: `h' `l' `ll'
* Type: `%cdiouxXpeEfgGaAs'

Note that CUDA's printf()will accept any combination of flag, width, precision, size and type, whether or not overall they form a valid format specifier. In other words, "%hd" will be accepted and printf will expect a double-precision variable in the corresponding location in the argument list.

### [B.17.2. Limitations](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "limitations)

Final formatting of the printf() output takes place on the host system. This means that the format string must be understood by the host-system's compiler and C library. Every effort has been made to ensure that the format specifiers supported by CUDA's printf function form a universal subset from the most common host compilers, but exact behavior will be host-OS-dependent.

As described in [Format Specifiers](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#format-specifiers), printf() will accept all combinations of valid flags and types. This is because it cannot determine what will and will not be valid on the host system where the final output is formatted. The effect of this is that output may be undefined if the program emits a format string which contains invalid combinations.

The printf() command can accept at most 32 arguments in addition to the format string. Additional arguments beyond this will be ignored, and the format specifier output as-is.

Owing to the differing size of the long type on 64-bit Windows platforms (four bytes on 64-bit Windows platforms, eight bytes on other 64-bit platforms), a kernel which is compiled on a non-Windows 64-bit machine but then run on a win64 machine will see corrupted output for all format strings which include "%ld". It is recommended that the compilation platform matches the execution platform to ensure safety.

The output buffer for printf() is set to a fixed size before kernel launch (see [Associated Host-Side API](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#associated-host-side-api)). It is circular and if more output is produced during kernel execution than can fit in the buffer, older output is overwritten. It is flushed only when one of these actions is performed:

* Kernel launch via <<<>>> or cuLaunchKernel() (at the start of the launch, and if the CUDA\_LAUNCH\_BLOCKING environment variable is set to 1, at the end of the launch as well),
* Synchronization via cudaDeviceSynchronize(), cuCtxSynchronize(), cudaStreamSynchronize(), cuStreamSynchronize(), cudaEventSynchronize(), or cuEventSynchronize(),
* Memory copies via any blocking version of cudaMemcpy\*() or cuMemcpy\*(),
* Module loading/unloading via cuModuleLoad() or cuModuleUnload(),
* Context destruction via cudaDeviceReset() or cuCtxDestroy().
* Prior to executing a stream callback added by cudaStreamAddCallback or cuStreamAddCallback.

Note that the buffer is not flushed automatically when the program exits. The user must call cudaDeviceReset() or cuCtxDestroy() explicitly, as shown in the examples below.

Internally printf() uses a shared data structure and so it is possible that calling printf() might change the order of execution of threads. In particular, a thread which calls printf() might take a longer execution path than one which does not call printf(), and that path length is dependent upon the parameters of the printf(). Note, however, that CUDA makes no guarantees of thread execution order except at explicit \_\_syncthreads() barriers, so it is impossible to tell whether execution order has been modified by printf() or by other scheduling behaviour in the hardware.

### [B.17.3. Associated Host-Side API](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "associated-host-side-api)

The following API functions get and set the size of the buffer used to transfer the printf() arguments and internal metadata to the host (default is 1 megabyte):

* cudaDeviceGetLimit(size\_t\* size,cudaLimitPrintfFifoSize)
* cudaDeviceSetLimit(cudaLimitPrintfFifoSize, size\_t size)

### [B.17.4. Examples](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "examples)

The following code sample:

#include <stdio.h>

\_\_global\_\_ void helloCUDA(float f)

{

printf("Hello thread %d, f=%f\n", threadIdx.x, f);

}

int main()

{

helloCUDA<<<1, 5>>>(1.2345f);

cudaDeviceSynchronize();

return 0;

}

will output:

Hello thread 2, f=1.2345

Hello thread 1, f=1.2345

Hello thread 4, f=1.2345

Hello thread 0, f=1.2345

Hello thread 3, f=1.2345

Notice how each thread encounters the printf() command, so there are as many lines of output as there were threads launched in the grid. As expected, global values (i.e., float f) are common between all threads, and local values (i.e., threadIdx.x) are distinct per-thread.

The following code sample:

#include <stdio.h>

\_\_global\_\_ void helloCUDA(float f)

{

if (threadIdx.x == 0)

printf("Hello thread %d, f=%f\n", threadIdx.x, f) ;

}

int main()

{

helloCUDA<<<1, 5>>>(1.2345f);

cudaDeviceSynchronize();

return 0;

}

will output:

Hello thread 0, f=1.2345

Self-evidently, the if() statement limits which threads will call printf, so that only a single line of output is seen.

### [B.18. Dynamic Global Memory Allocation and Operations](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "dynamic-global-memory-allocation-and-operations)

Dynamic global memory allocation and operations are only supported by devices of compute capability 2.x and higher.

void\* malloc(size\_t size);

void free(void\* ptr);

allocate and free memory dynamically from a fixed-size heap in global memory.

void\* memcpy(void\* dest, const void\* src, size\_t size);

copy size bytes from the memory location pointed by src to the memory location pointed by dest.

void\* memset(void\* ptr, int value, size\_t size);

set size bytes of memory block pointed by ptr to value (interpreted as an unsigned char).

The CUDA in-kernel malloc() function allocates at least size bytes from the device heap and returns a pointer to the allocated memory or NULL if insufficient memory exists to fulfill the request. The returned pointer is guaranteed to be aligned to a 16-byte boundary.

The CUDA in-kernel free() function deallocates the memory pointed to by ptr, which must have been returned by a previous call to malloc(). If ptr is NULL, the call to free() is ignored. Repeated calls to free() with the same ptr has undefined behavior.

The memory allocated by a given CUDA thread via malloc() remains allocated for the lifetime of the CUDA context, or until it is explicitly released by a call to free(). It can be used by any other CUDA threads even from subsequent kernel launches. Any CUDA thread may free memory allocated by another thread, but care should be taken to ensure that the same pointer is not freed more than once.

### [B.18.1. Heap Memory Allocation](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "heap-memory-allocation)

The device memory heap has a fixed size that must be specified before any program using malloc() or free() is loaded into the context. A default heap of eight megabytes is allocated if any program uses malloc() without explicitly specifying the heap size.

The following API functions get and set the heap size:

* cudaDeviceGetLimit(size\_t\* size, cudaLimitMallocHeapSize)
* cudaDeviceSetLimit(cudaLimitMallocHeapSize, size\_t size)

The heap size granted will be at least size bytes. cuCtxGetLimit()and cudaDeviceGetLimit() return the currently requested heap size.

The actual memory allocation for the heap occurs when a module is loaded into the context, either explicitly via the CUDA driver API (see [Module](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#module)), or implicitly via the CUDA runtime API (see [CUDA C Runtime](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#cuda-c-runtime)). If the memory allocation fails, the module load will generate a CUDA\_ERROR\_SHARED\_OBJECT\_INIT\_FAILED error.

Heap size cannot be changed once a module load has occurred and it does not resize dynamically according to need.

Memory reserved for the device heap is in addition to memory allocated through host-side CUDA API calls such as cudaMalloc().

### [B.18.2. Interoperability with Host Memory API](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "interoperability-host-memory-api)

Memory allocated via malloc() cannot be freed using the runtime (i.e., by calling any of the free memory functions from [Device Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#device-memory)).

Similarly, memory allocated via the runtime (i.e., by calling any of the memory allocation functions from [Device Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#device-memory)) cannot be freed via free().

### [B.18.3. Examples](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "examples-per-thread)

### [B.18.3.1. Per Thread Allocation](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "per-thread-allocation)

The following code sample:

#include <stdlib.h>

#include <stdio.h>

\_\_global\_\_ void mallocTest()

{

size\_t size = 123;

char\* ptr = (char\*)malloc(size);

memset(ptr, 0, size);

printf("Thread %d got pointer: %p\n", threadIdx.x, ptr);

free(ptr);

}

int main()

{

// Set a heap size of 128 megabytes. Note that this must

// be done before any kernel is launched.

cudaDeviceSetLimit(cudaLimitMallocHeapSize, 128\*1024\*1024);

mallocTest<<<1, 5>>>();

cudaDeviceSynchronize();

return 0;

}

will output:

Thread 0 got pointer: 00057020

Thread 1 got pointer: 0005708c

Thread 2 got pointer: 000570f8

Thread 3 got pointer: 00057164

Thread 4 got pointer: 000571d0

Notice how each thread encounters the malloc() and memset() commands and so receives and initializes its own allocation. (Exact pointer values will vary: these are illustrative.)

### [B.18.3.2. Per Thread Block Allocation](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "per-thread-block-allocation)

#include <stdlib.h>

\_\_global\_\_ void mallocTest()

{

\_\_shared\_\_ int\* data;

// The first thread in the block does the allocation and initialization

// and then shares the pointer with all other threads through shared memory,

// so that access can easily be coalesced.

// 64 bytes per thread are allocated.

if (threadIdx.x == 0) {

size\_t size = blockDim.x \* 64;

data = (int\*)malloc(size);

memset(data, 0, size);

}

\_\_syncthreads();

// Check for failure

if (data == NULL)

return;

// Threads index into the memory, ensuring coalescence

int\* ptr = data;

for (int i = 0; i < 64; ++i)

ptr[i \* blockDim.x + threadIdx.x] = threadIdx.x;

// Ensure all threads complete before freeing

\_\_syncthreads();

// Only one thread may free the memory!

if (threadIdx.x == 0)

free(data);

}

int main()

{

cudaDeviceSetLimit(cudaLimitMallocHeapSize, 128\*1024\*1024);

mallocTest<<<10, 128>>>();

cudaDeviceSynchronize();

return 0;

}

### [B.18.3.3. Allocation Persisting Between Kernel Launches](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "allocation-persisting-kernel-launches)

#include <stdlib.h>

#include <stdio.h>

#define NUM\_BLOCKS 20

\_\_device\_\_ int\* dataptr[NUM\_BLOCKS]; // Per-block pointer

\_\_global\_\_ void allocmem()

{

// Only the first thread in the block does the allocation

// since we want only one allocation per block.

if (threadIdx.x == 0)

dataptr[blockIdx.x] = (int\*)malloc(blockDim.x \* 4);

\_\_syncthreads();

// Check for failure

if (dataptr[blockIdx.x] == NULL)

return;

// Zero the data with all threads in parallel

dataptr[blockIdx.x][threadIdx.x] = 0;

}

// Simple example: store thread ID into each element

\_\_global\_\_ void usemem()

{

int\* ptr = dataptr[blockIdx.x];

if (ptr != NULL)

ptr[threadIdx.x] += threadIdx.x;

}

// Print the content of the buffer before freeing it

\_\_global\_\_ void freemem()

{

int\* ptr = dataptr[blockIdx.x];

if (ptr != NULL)

printf("Block %d, Thread %d: final value = %d\n",

blockIdx.x, threadIdx.x, ptr[threadIdx.x]);

// Only free from one thread!

if (threadIdx.x == 0)

free(ptr);

}

int main()

{

cudaDeviceSetLimit(cudaLimitMallocHeapSize, 128\*1024\*1024);

// Allocate memory

allocmem<<< NUM\_BLOCKS, 10 >>>();

// Use memory

usemem<<< NUM\_BLOCKS, 10 >>>();

usemem<<< NUM\_BLOCKS, 10 >>>();

usemem<<< NUM\_BLOCKS, 10 >>>();

// Free memory

freemem<<< NUM\_BLOCKS, 10 >>>();

cudaDeviceSynchronize();

return 0;

}

### [B.19. Execution Configuration](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "execution-configuration)

Any call to a \_\_global\_\_ function must specify the execution configuration for that call. The execution configuration defines the dimension of the grid and blocks that will be used to execute the function on the device, as well as the associated stream (see [CUDA C Runtime](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#cuda-c-runtime) for a description of streams).

The execution configuration is specified by inserting an expression of the form <<< Dg, Db, Ns, S >>> between the function name and the parenthesized argument list, where:

* Dg is of type dim3 (see [dim3](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#dim3)) and specifies the dimension and size of the grid, such that Dg.x \* Dg.y \* Dg.z equals the number of blocks being launched;
* Db is of type dim3 (see [dim3](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#dim3)) and specifies the dimension and size of each block, such that Db.x \* Db.y \* Db.z equals the number of threads per block;
* Ns is of type size\_t and specifies the number of bytes in shared memory that is dynamically allocated per block for this call in addition to the statically allocated memory; this dynamically allocated memory is used by any of the variables declared as an external array as mentioned in [\_\_shared\_\_](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#shared); Ns is an optional argument which defaults to 0;
* S is of type cudaStream\_t and specifies the associated stream; S is an optional argument which defaults to 0.

As an example, a function declared as

\_\_global\_\_ void Func(float\* parameter);

must be called like this:

Func<<< Dg, Db, Ns >>>(parameter);

The arguments to the execution configuration are evaluated before the actual function arguments.

The function call will fail if Dg or Db are greater than the maximum sizes allowed for the device as specified in [Compute Capabilities](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compute-capabilities), or if Ns is greater than the maximum amount of shared memory available on the device, minus the amount of shared memory required for static allocation.

### [B.20. Launch Bounds](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "launch-bounds)

As discussed in detail in [Multiprocessor Level](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#multiprocessor-level), the fewer registers a kernel uses, the more threads and thread blocks are likely to reside on a multiprocessor, which can improve performance.

Therefore, the compiler uses heuristics to minimize register usage while keeping register spilling (see [Device Memory Accesses](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#device-memory-accesses)) and instruction count to a minimum. An application can optionally aid these heuristics by providing additional information to the compiler in the form of launch bounds that are specified using the \_\_launch\_bounds\_\_() qualifier in the definition of a \_\_global\_\_ function:

\_\_global\_\_ void

\_\_launch\_bounds\_\_(maxThreadsPerBlock, minBlocksPerMultiprocessor)

MyKernel(...)

{

...

}

* maxThreadsPerBlock specifies the maximum number of threads per block with which the application will ever launch MyKernel(); it compiles to the .maxntidPTX directive;
* minBlocksPerMultiprocessor is optional and specifies the desired minimum number of resident blocks per multiprocessor; it compiles to the .minnctapersmPTX directive.

If launch bounds are specified, the compiler first derives from them the upper limit L on the number of registers the kernel should use to ensure that minBlocksPerMultiprocessor blocks (or a single block if minBlocksPerMultiprocessor is not specified) of maxThreadsPerBlock threads can reside on the multiprocessor (see [Hardware Multithreading](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#hardware-multithreading) for the relationship between the number of registers used by a kernel and the number of registers allocated per block). The compiler then optimizes register usage in the following way:

* If the initial register usage is higher than L, the compiler reduces it further until it becomes less or equal to L, usually at the expense of more local memory usage and/or higher number of instructions;
* If the initial register usage is lower than L
  + If maxThreadsPerBlock is specified and minBlocksPerMultiprocessor is not, the compiler uses maxThreadsPerBlock to determine the register usage thresholds for the transitions between n and n+1 resident blocks (i.e., when using one less register makes room for an additional resident block as in the example of [Multiprocessor Level](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#multiprocessor-level)) and then applies similar heuristics as when no launch bounds are specified;
  + If both minBlocksPerMultiprocessor and maxThreadsPerBlock are specified, the compiler may increase register usage as high as L to reduce the number of instructions and better hide single thread instruction latency.

A kernel will fail to launch if it is executed with more threads per block than its launch bound maxThreadsPerBlock.

Optimal launch bounds for a given kernel will usually differ across major architecture revisions. The sample code below shows how this is typically handled in device code using the \_\_CUDA\_ARCH\_\_ macro introduced in [Application Compatibility](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#application-compatibility)

#define THREADS\_PER\_BLOCK 256

#if \_\_CUDA\_ARCH\_\_ >= 200

#define MY\_KERNEL\_MAX\_THREADS (2 \* THREADS\_PER\_BLOCK)

#define MY\_KERNEL\_MIN\_BLOCKS 3

#else

#define MY\_KERNEL\_MAX\_THREADS THREADS\_PER\_BLOCK

#define MY\_KERNEL\_MIN\_BLOCKS 2

#endif

// Device code

\_\_global\_\_ void

\_\_launch\_bounds\_\_(MY\_KERNEL\_MAX\_THREADS, MY\_KERNEL\_MIN\_BLOCKS)

MyKernel(...)

{

...

}

In the common case where MyKernel is invoked with the maximum number of threads per block (specified as the first parameter of \_\_launch\_bounds\_\_()), it is tempting to use MY\_KERNEL\_MAX\_THREADS as the number of threads per block in the execution configuration:

// Host code

MyKernel<<<blocksPerGrid, MY\_KERNEL\_MAX\_THREADS>>>(...);

This will not work however since \_\_CUDA\_ARCH\_\_ is undefined in host code as mentioned in [Application Compatibility](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#application-compatibility), so MyKernel will launch with 256 threads per block even when \_\_CUDA\_ARCH\_\_ is greater or equal to 200. Instead the number of threads per block should be determined:

* Either at compile time using a macro that does not depend on \_\_CUDA\_ARCH\_\_, for example
* // Host code

MyKernel<<<blocksPerGrid, THREADS\_PER\_BLOCK>>>(...);

* Or at runtime based on the compute capability
* // Host code
* cudaGetDeviceProperties(&deviceProp, device);
* int threadsPerBlock =
* (deviceProp.major >= 2 ?
* 2 \* THREADS\_PER\_BLOCK : THREADS\_PER\_BLOCK);

MyKernel<<<blocksPerGrid, threadsPerBlock>>>(...);

Register usage is reported by the --ptxas options=-v compiler option. The number of resident blocks can be derived from the occupancy reported by the CUDA profiler (see [Device Memory Accesses](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#device-memory-accesses)for a definition of occupancy).

Register usage can also be controlled for all \_\_global\_\_ functions in a file using the maxrregcount compiler option. The value of maxrregcount is ignored for functions with launch bounds.

### [B.21. #pragma unroll](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "pragma-unroll)

By default, the compiler unrolls small loops with a known trip count. The #pragma unroll directive however can be used to control unrolling of any given loop. It must be placed immediately before the loop and only applies to that loop. It is optionally followed by a number that specifies how many times the loop must be unrolled.

For example, in this code sample:

#pragma unroll 5

for (int i = 0; i < n; ++i)

the loop will be unrolled 5 times. The compiler will also insert code to ensure correctness (in the example above, to ensure that there will only be n iterations if n is less than 5, for example). It is up to the programmer to make sure that the specified unroll number gives the best performance.

#pragma unroll 1 will prevent the compiler from ever unrolling a loop.

If no number is specified after #pragma unroll, the loop is completely unrolled if its trip count is constant, otherwise it is not unrolled at all.

### [B.22. SIMD Video Instructions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "simd-video)

PTX ISA version 3.0 includes SIMD (Single Instruction, Multiple Data) video instructions which operate on pairs of 16-bit values and quads of 8-bit values. These are available on devices of compute capability 3.0.

The SIMD video instructions are:

* vadd2, vadd4
* vsub2, vsub4
* vavrg2, vavrg4
* vabsdiff2, vabsdiff4
* vmin2, vmin4
* vmax2, vmax4
* vset2, vset4

PTX instructions, such as the SIMD video instructions, can be included in CUDA programs by way of the assembler, asm(), statement.

The basic syntax of an asm() statement is:

asm("template-string" : "constraint"(output) : "constraint"(input)"));

An example of using the vabsdiff4 PTX instruction is:

asm("vabsdiff4.u32.u32.u32.add" " %0, %1, %2, %3;": "=r" (result):"r" (A), "r" (B), "r" (C));

This uses the vabsdiff4 instruction to compute an integer quad byte SIMD sum of absolute differences. The absolute difference value is computed for each byte of the unsigned integers A and B in SIMD fashion. The optional accumulate operation (.add) is specified to sum these differences.

Refer to the document "Using Inline PTX Assembly in CUDA" for details on using the assembly statement in your code. Refer to the PTX ISA documentation ("Parallel Thread Execution ISA Version 3.0" for example) for details on the PTX instructions for the version of PTX that you are using.

## [C. CUDA Dynamic Parallelism](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "cuda-dynamic-parallelism)

### [C.1. Introduction](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "introduction-cuda-dynamic-parallelism)

### [C.1.1. Overview](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "overview)

Dynamic Parallelism is an extension to the CUDA programming model enabling a CUDA kernel to create and synchronize with new work directly on the GPU. The creation of parallelism dynamically at whichever point in a program that it is needed offers exciting new capabilities.

The ability to create work directly from the GPU can reduce the need to transfer execution control and data between host and device, as launch configuration decisions can now be made at runtime by threads executing on the device. Additionally, data-dependent parallel work can be generated inline within a kernel at run-time, taking advantage of the GPU's hardware schedulers and load balancers dynamically and adapting in response to data-driven decisions or workloads. Algorithms and programming patterns that had previously required modifications to eliminate recursion, irregular loop structure, or other constructs that do not fit a flat, single-level of parallelism may more transparently be expressed.

This document describes the extended capabilities of CUDA which enable Dynamic Parallelism, including the modifications and additions to the CUDA programming model necessary to take advantage of these, as well as guidelines and best practices for exploiting this added capacity.

Dynamic Parallelism is only supported by devices of compute capability 3.5 and higher.

### [C.1.2. Glossary](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "glossary)

Definitions for terms used in this guide.

Grid

A Grid is a collection of Threads. Threads in a Grid execute a Kernel Function and are divided into Thread Blocks.

Thread Block

A Thread Block is a group of threads which execute on the same multiprocessor (SMX). Threads within a Thread Block have access to shared memory and can be explicitly synchronized.

Kernel Function

A Kernel Function is an implicitly parallel subroutine that executes under the CUDA execution and memory model for every Thread in a Grid.

Host

The Host refers to the execution environment that initially invoked CUDA. Typically the thread running on a system's CPU processor.

Parent

A Parent Thread, Thread Block, or Grid is one that has launched new grid(s), the Child Grid(s). The Parent is not considered completed until all of its launched Child Grids have also completed.

Child

A Child thread, block, or grid is one that has been launched by a Parent grid. A Child grid must complete before the Parent Thread, Thread Block, or Grid are considered complete.

Thread Block Scope

Objects with Thread Block Scope have the lifetime of a single Thread Block. They only have defined behavior when operated on by Threads in the Thread Block that created the object and are destroyed when the Thread Block that created them is complete.

Device Runtime

The Device Runtime refers to the runtime system and APIs available to enable Kernel Functions to use Dynamic Parallelism.

### [C.2. Execution Environment and Memory Model](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "execution-environment-and-memory-model)

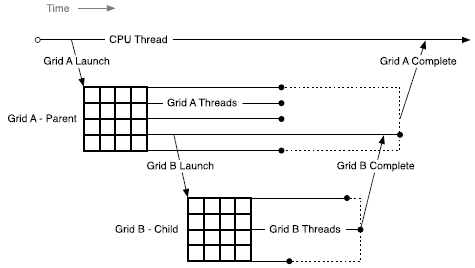
### [C.2.1. Execution Environment](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "execution-environment)

The CUDA execution model is based on primitives of threads, thread blocks, and grids, with kernel functions defining the program executed by individual threads within a thread block and grid. When a kernel function is invoked the grid's properties are described by an execution configuration, which has a special syntax in CUDA. Support for dynamic parallelism in CUDA extends the ability to configure, launch, and synchronize upon new grids to threads that are running on the device.

### [C.2.1.1. Parent and Child Grids](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "parent-and-child-grids)

A device thread that configures and launches a new grid belongs to the parent grid, and the grid created by the invocation is a child grid.

The invocation and completion of child grids is properly nested, meaning that the parent grid is not considered complete until all child grids created by its threads have completed. Even if the invoking threads do not explicitly synchronize on the child grids launched, the runtime guarantees an implicit synchronization between the parent and child.

Figure 12. Parent-Child Launch Nesting

### [C.2.1.2. Scope of CUDA Primitives](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "scope-of-cuda-primitives)

On both host and device, the CUDA runtime offers an API for launching kernels, for waiting for launched work to complete, and for tracking dependencies between launches via streams and events. On the host system, the state of launches and the CUDA primitives referencing streams and events are shared by all threads within a process; however processes execute independently and may not share CUDA objects.

A similar hierarchy exists on the device: launched kernels and CUDA objects are visible to all threads in a thread block, but are independent between thread blocks. This means for example that a stream may be created by one thread and used by any other thread in the same thread block, but may not be shared with threads in any other thread block.

### [C.2.1.3. Synchronization](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "synchronization)

CUDA runtime operations from any thread, including kernel launches, are visible across a thread block. This means that an invoking thread in the parent grid may perform synchronization on the grids launched by that thread, by other threads in the thread block, or on streams created within the same thread block. Execution of a thread block is not considered complete until all launches by all threads in the block have completed. If all threads in a block exit before all child launches have completed, a synchronization operation will automatically be triggered.

### [C.2.1.4. Streams and Events](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "streams-and-events)

CUDA Streams and Events allow control over dependencies between grid launches: grids launched into the same stream execute in-order, and events may be used to create dependencies between streams. Streams and events created on the device serve this exact same purpose.

Streams and events created within a grid exist within thread block scope but have undefined behavior when used outside of the thread block where they were created. As described above, all work launched by a thread block is implicitly synchronized when the block exits; work launched into streams is included in this, with all dependencies resolved appropriately. The behavior of operations on a stream that has been modified outside of thread block scope is undefined.

Streams and events created on the host have undefined behavior when used within any kernel, just as streams and events created by a parent grid have undefined behavior if used within a child grid.

### [C.2.1.5. Ordering and Concurrency](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "ordering-and-concurrency)

The ordering of kernel launches from the device runtime follows CUDA Stream ordering semantics. Within a thread block, all kernel launches into the same stream are executed in-order. With multiple threads in the same thread block launching into the same stream, the ordering within the stream is dependent on the thread scheduling within the block, which may be controlled with synchronization primitives such as \_\_syncthreads().

Note that because streams are shared by all threads within a thread block, the implicit NULL stream is also shared. If multiple threads in a thread block launch into the implicit stream, then these launches will be executed in-order. If concurrency is desired, explicit named streams should be used.

Dynamic Parallelism enables concurrency to be expressed more easily within a program; however, the device runtime introduces no new concurrency guarantees within the CUDA execution model. There is no guarantee of concurrent execution between any number of different thread blocks on a device.

The lack of concurrency guarantee extends to parent thread blocks and their child grids. When a parent thread block launches a child grid, the child is not guaranteed to begin execution until the parent thread block reaches an explicit synchronization point (e.g. cudaDeviceSynchronize()).

While concurrency will often easily be achieved, it may vary as a function of deviceconfiguration, application workload, and runtime scheduling. It is therefore unsafe to depend upon any concurrency between different thread blocks.

### [C.2.1.6. Device Management](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "device-management)

There is no multi-GPU support from the device runtime; the device runtime is only capable of operating on the device upon which it is currently executing. It is permitted, however, to query properties for any CUDA capable device in the system.

### [C.2.2. Memory Model](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "memory-model)

Parent and child grids share the same global and constant memory storage, but have distinct local and shared memory.

### [C.2.2.1. Coherence and Consistency](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "coherence-and-consistency)

### [C.2.2.1.1. Global Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "global-memory)

Parent and child grids have coherent access to global memory, with weak consistency guarantees between child and parent. There are two points in the execution of a child grid when its view of memory is fully consistent with the parent thread: when the child grid is invoked by the parent, and when the child grid completes as signaled by a synchronization API invocation in the parent thread.

All global memory operations in the parent thread prior to the child grid's invocation are visible to the child grid. All memory operations of the child grid are visible to the parent after the parent has synchronized on the child grid's completion.

In the following example, the child grid executing child\_launch is only guaranteed to see the modifications to data made before the child grid was launched. Since thread 0 of the parent is performing the launch, the child will be consistent with the memory seen by thread 0 of the parent. Due to the first \_\_syncthreads() call, the child will see data[0]=0, data[1]=1, ..., data[255]=255 (without the \_\_syncthreads() call, only data[0] would be guaranteed to be seen by the child). When the child grid returns, thread 0 is guaranteed to see modifications made by the threads in its child grid. Those modifications become available to the other threads of the parent grid only after the second \_\_syncthreads() call:

\_\_global\_\_ void child\_launch(int \*data) {

data[threadIdx.x] = data[threadIdx.x]+1;

}

\_\_global\_\_ void parent\_launch(int \*data) {

data[threadIdx.x] = threadIdx.x;

\_\_syncthreads();

if (threadIdx.x == 0) {

child\_launch<<< 1, 256 >>>(data);

cudaDeviceSynchronize();

}

\_\_syncthreads();

}

void host\_launch(int \*data) {

parent\_launch<<< 1, 256 >>>(data);

}

### [C.2.2.1.2. Zero Copy Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "zero-copy-memory)

Zero-copy system memory has identical coherence and consistency guarantees to global memory, and follows the semantics detailed above. A kernel may not allocate or free zero-copy memory, but may use pointers to zero-copy passed in from the host program.

### [C.2.2.1.3. Constant Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "constant-memory)

Constants are immutable and may not be modified from the device, even between parent and child launches. That is to say, the value of all \_\_constant\_\_ variables must be set from the host prior to launch. Constant memory is inherited automatically by all child kernels from their respective parents.

Taking the address of a constant memory object from within a kernel thread has the same semantics as for all CUDA programs, and passing that pointer from parent to child or from a child to parent is naturally supported.

### [C.2.2.1.4. Shared and Local Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "shared-and-local-memory)

Shared and Local memory is private to a thread block or thread, respectively, and is not visible or coherent between parent and child. Behavior is undefined when an object in one of these locations is referenced outside of the scope within which it belongs, and may cause an error.

The NVIDIA compiler will attempt to warn if it can detect that a pointer to local or shared memory is being passed as an argument to a kernel launch. At runtime, the programmer may use the \_\_isGlobal() intrinsic to determine whether a pointer references global memory and so may safely be passed to a child launch.

Note that calls to cudaMemcpy\*Async() or cudaMemset\*Async() may invoke new child kernels on the device in order to preserve stream semantics. As such, passing shared or local memory pointers to these APIs is illegal and will return an error.

### [C.2.2.1.5. Local Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "local-memory)

Local memory is private storage for an executing thread, and is not visible outside of that thread. It is illegal to pass a pointer to local memory as a launch argument when launching a child kernel. The result of dereferencing such a local memory pointer from a child will be undefined.

For example the following is illegal, with undefined behavior if x\_array is accessed by child\_launch:

int x\_array[10]; // Creates x\_array in parent's local memory

child\_launch<<< 1, 1 >>>(x\_array);

It is sometimes difficult for a programmer to be aware of when a variable is placed into local memory by the compiler. As a general rule, all storage passed to a child kernel should be allocated explicitly from the global-memory heap, either with cudaMalloc(), new() or by declaring \_\_device\_\_ storage at global scope. For example:

// Correct - "value" is global storage

\_\_device\_\_ int value;

\_\_device\_\_ void x() {

value = 5;

child<<< 1, 1 >>>(&value);

}

// Invalid - "value" is local storage

\_\_device\_\_ void y() {

int value = 5;

child<<< 1, 1 >>>(&value);

}

### [C.2.2.1.6. Texture Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "texture-memory-cdp)

Writes to the global memory region over which a texture is mapped are incoherent with respect to texture accesses. Coherence for texture memory is enforced at the invocation of a child grid and when a child grid completes. This means that writes to memory prior to a child kernel launch are reflected in texture memory accesses of the child. Similarly, writes to memory by a child will be reflected in the texture memory accesses by a parent, but only after the parent synchronizes on the child's completion. Concurrent accesses by parent and child may result in inconsistent data.

### [C.3. Programming Interface](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "programming-interface-cdp)

### [C.3.1. CUDA C/C++ Reference](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "cuda-c-cplusplus)

This section describes changes and additions to the CUDA C/C++ language extensions for supporting Dynamic Parallelism.

The language interface and API available to CUDA kernels using CUDA C/C++ for Dynamic Parallelism, referred to as the Device Runtime, is substantially like that of the CUDA Runtime API available on the host. Where possible the syntax and semantics of the CUDA Runtime API have been retained in order to facilitate ease of code reuse for routines that may run in either the host or device environments.

As with all code in CUDA C/C++, the APIs and code outlined here is per-thread code. This enables each thread to make unique, dynamic decisions regarding what kernel or operation to execute next. There are no synchronization requirements between threads within a block to execute any of the provided device runtime APIs, which enables the device runtime API functions to be called in arbitrarily divergent kernel code without deadlock.

### [C.3.1.1. Device-Side Kernel Launch](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "device-side-kernel-launch)

Kernels may be launched from the device using the standard CUDA <<< >>> syntax:

kernel\_name<<< Dg, Db, Ns, S >>>([kernel arguments]);

* Dg is of type dim3 and specifies the dimensions and size of the grid
* Db is of type dim3 and specifies the dimensions and size of each thread block
* Ns is of type size\_t and specifies the number of bytes of shared memory that is dynamically allocated per thread block for this call and addition to statically allocated memory. Ns is an optional argument that defaults to 0.
* S is of type cudaStream\_t and specifies the stream associated with this call. The stream must have been allocated in the same thread block where the call is being made. S is an optional argument that defaults to 0.

### [C.3.1.1.1. Launches are Asynchronous](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "launches-are-asynchronous)

Identical to host-side launches, all device-side kernel launches are asynchronous with respect to the launching thread. That is to say, the <<<>>> launch command will return immediately and the launching thread will continue to execute until it hits an explicit launch-synchronization point such as cudaDeviceSynchronize(). The grid launch is posted to the device and will execute independently of the parent thread. The child grid may begin execution at any time after launch, but is not guaranteed to begin execution until the launching thread reaches an explicit launch-synchronization point.

### [C.3.1.1.2. Launch Environment Configuration](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "launch-environment-configuration)

All global device configuration settings (e.g., shared memory and L1 cache size as returned from cudaDeviceGetCacheConfig(), and device limits returned from cudaDeviceGetLimit()) will be inherited from the parent. That is to say if, when the parent is launched, execution is configured globally for 16k of shared memory and 48k of L1 cache, then the child's execution state will be configured identically. Likewise, device limits such as stack size will remain as-configured.

For host-launched kernels, per-kernel configurations set from the host will take precedence over the global setting. These configurations will be used when the kernel is launched from the device as well. It is not possible to reconfigure a kernel's environment from the device.

### [C.3.1.1.3. Launch from \_\_host\_\_ \_\_device\_\_ Functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "launch-from-host-device-functions)

Although the device runtime enables kernel launches from either the host or device, kernel launches from \_\_host\_\_ \_\_device\_\_ functions are unsupported. The compiler will fail to compile if a \_\_host\_\_ device\_\_ function is used to launch a kernel.

### [C.3.1.2. Streams](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "streams-cdp)

Both named and unnamed (NULL) streams are available from the device runtime. Named streams may be used by any thread within a thread-block, but stream handles may not be passed to other blocks or child/parent kernels. In other words, a stream should be treated as private to the block in which it is created. Stream handles are not guaranteed to be unique between blocks, so using a stream handle within a block that did not allocate it will result in undefined behavior.

Similar to host-side launch, work launched into separate streams may run concurrently, but actual concurrency is not guaranteed. Programs that depend upon concurrency between child kernels are not supported by the CUDA programming model and will have undefined behavior.

The host-side NULL stream's cross-stream barrier semantic is not supported on the device (see below for details). In order to retain semantic compatibility with the host runtime, all device streams must be created using the cudaStreamCreateWithFlags() API, passing the cudaStreamNonBlocking flag. The cudaStreamCreate() call is a host-runtime- only API and will fail to compile for the device.

As cudaStreamSynchronize() and cudaStreamQuery() are unsupported by the device runtime, cudaDeviceSynchronize() should be used instead when the application needs to know that stream-launched child kernels have completed.

### [C.3.1.2.1. The Implicit (NULL) Stream](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "implicit-null-stream)

Within a host program, the unnamed (NULL) stream has additional barrier synchronization semantics with other streams (see [Default Stream](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#default-stream) for details). The device runtime offers a single implicit, unnamed stream shared between all threads in a block, but as all named streams must be created with the cudaStreamNonBlocking flag, work launched into the NULL stream will not insert an implicit dependency on pending work in any other streams.

### [C.3.1.3. Events](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "events-cdp)

Only the inter-stream synchronization capabilities of CUDA events are supported. This means that cudaStreamWaitEvent() is supported, but cudaEventSynchronize(), cudaEventElapsedTime(), and cudaEventQuery() are not. As cudaEventElapsedTime() is not supported, cudaEvents must be created via cudaEventCreateWithFlags(), passing the cudaEventDisableTiming flag.

As for all device runtime objects, event objects may be shared between all threads withinthe thread-block which created them but are local to that block and may not be passed to other kernels, or between blocks within the same kernel. Event handles are not guaranteed to be unique between blocks, so using an event handle within a block that did not create it will result in undefined behavior.

### [C.3.1.4. Synchronization](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "synchronization-programming-interface)

The cudaDeviceSynchronize() function will synchronize on all work launched by any thread in the thread-block up to the point where cudaDeviceSynchronize() was called. Note that cudaDeviceSynchronize() may be called from within divergent code (see [Block Wide Synchronization](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#block-wide-synchronization)).

It is up to the program to perform sufficient additional inter-thread synchronization, for example via a call to \_\_syncthreads(), if the calling thread is intended to synchronize with child grids invoked from other threads.

### [C.3.1.4.1. Block Wide Synchronization](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "block-wide-synchronization)

The cudaDeviceSynchronize() function does not imply intra-block synchronization. In particular, without explicit synchronization via a \_\_syncthreads() directive the calling thread can make no assumptions about what work has been launched by any thread other than itself. For example if multiple threads within a block are each launching work and synchronization is desired for all this work at once (perhaps because of event-based dependencies), it is up to the program to guarantee that this work is submitted by all threads before calling cudaDeviceSynchronize().

Because the implementation is permitted to synchronize on launches from any thread in the block, it is quite possible that simultaneous calls to cudaDeviceSynchronize() by multiple threads will drain all work in the first call and then have no effect for the later calls.

### [C.3.1.5. Device Management](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "device-management-programming)

Only the device on which a kernel is running will be controllable from that kernel. This means that device APIs such as cudaSetDevice() are not supported by the device runtime. The active device as seen from the GPU (returned from cudaGetDevice()) will have the same device number as seen from the host system. The cudaGetDeviceProperty() call may request information about another device as this API allows specification of a device ID as a parameter of the call. Note that the catch-all cudaGetDeviceProperties() API is not offered by the device runtime - properties must be queried individually.

### [C.3.1.6. Memory Declarations](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "memory-declarations)

### [C.3.1.6.1. Device and Constant Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "device-and-constant-memory)

Memory declared at file scope with \_\_device\_\_ or \_\_constant\_\_ qualifiers behave identically when using the device runtime. All kernels may read or write device variables, whether the kernel was initially launched by the host or device runtime. Equivalently, all kernels will have the same view of \_\_constant\_\_s as declared at the module scope.

### [C.3.1.6.2. Textures & Surfaces](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "textures-and-surfaces)

CUDA supports dynamically created texture and surface objects[1](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "fntarg_6), where a texture reference may be created on the host, passed to a kernel, used by that kernel, and then destroyed from the host. The device runtime does not allow creation or destruction of texture or surface objects from within device code, but texture and surface objects created from the host may be used and passed around freely on the device. Regardless of where they are created, dynamically created texture objects are always valid and may be passed to child kernels from a parent.

Note: The device runtime does not support legacy module-scope (i.e., Fermi-style) textures and surfaces within a kernel launched from the device. Module-scope (legacy) textures may be created from the host and used in device code as for any kernel, but may only be used by a top-level kernel (i.e., the one which is launched from the host).

### [C.3.1.6.3. Shared Memory Variable Declarations](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "shared-memory-variable-declarations)

In CUDA C/C++ shared memory can be declared either as a statically sized file-scope or function-scoped variable, or as an extern variable with the size determined at runtime by the kernel's caller via a launch configuration argument. Both types of declarations are valid under the device runtime.

\_\_global\_\_ void permute(int n, int \*data) {

extern \_\_shared\_\_ int smem[];

if (n <= 1)

return;

smem[threadIdx.x] = data[threadIdx.x];

\_\_syncthreads();

permute\_data(smem, n);

\_\_syncthreads();

// Write back to GMEM since we can't pass SMEM to children.

data[threadIdx.x] = smem[threadIdx.x];

\_\_syncthreads();

if (threadIdx.x == 0) {

permute<<< 1, 256, n/2\*sizeof(int) >>>(n/2, data);

permute<<< 1, 256, n/2\*sizeof(int) >>>(n/2, data+n/2);

}

}

void host\_launch(int \*data) {

permute<<< 1, 256, 256\*sizeof(int) >>>(256, data);

}

### [C.3.1.6.4. Symbol Addresses](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "symbol-addresses)

Device-side symbols (i.e., those marked \_\_device\_\_) may be referenced from within a kernel simply via the & operator, as all global-scope device variables are in the kernel's visible address space. This also applies to \_\_constant\_\_ symbols, although in this case the pointer will reference read-only data.

Given that device-side symbols can be referenced directly, those CUDA runtime APIs which reference symbols (e.g., cudaMemcpyToSymbol() or cudaGetSymbolAddress()) are redundant and hence not supported by the device runtime. Note this implies that constant data cannot be altered from within a running kernel, even ahead of a child kernel launch, as references to \_\_constant\_\_ space are read-only.

### [C.3.1.7. API Errors and Launch Failures](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "api-errors-and-launch-failures)

As usual for the CUDA runtime, any function may return an error code. The last error code returned is recorded and may be retrieved via the cudaGetLastError() call. Errors are recorded per-thread, so that each thread can identify the most recent error that it has generated. The error code is of type cudaError\_t.

Similar to a host-side launch, device-side launches may fail for many reasons (invalid arguments, etc). The user must call cudaGetLastError() to determine if a launch generated an error, however lack of an error after launch does not imply the child kernel completed successfully.

For device-side exceptions, e.g., access to an invalid address, an error in a child grid will be returned to the host instead of being returned by the parent's call to cudaDeviceSynchronize().

### [C.3.1.7.1. Launch Setup APIs](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "launch-setup-apis)

Kernel launch is a system-level mechanism exposed through the device runtime library, and as such is available directly from PTX via the underlying cudaGetParameterBuffer() and cudaLaunchDevice() APIs. It is permitted for a CUDA application to call these APIs itself, with the same requirements as for PTX. In both cases, the user is then responsible for correctly populating all necessary data structures in the correct format according to specification. Backwards compatibility is guaranteed in these data structures.

As with host-side launch, the device-side operator <<<>>> maps to underlying kernel launch APIs. This is so that users targeting PTX will be able to enact a launch, and so that the compiler front-end can translate <<<>>> into these calls.

| Table 4. New Device-only Launch Implementation Functions | |
| --- | --- |
| **Runtime API Launch Functions** | **Description of Difference From Host Runtime Behaviour (behaviour is identical if no description)** |
| cudaGetParameterBuffer | Generated automatically from <<<>>>. Note different API to host equivalent. |
| cudaLaunchDevice | Generated automatically from <<<>>>. Note different API to host equivalent. |

The APIs for these launch functions are different to those of the CUDA Runtime API, and are defined as follows:

extern device cudaError\_t cudaGetParameterBuffer(void \*\*params);

extern \_\_device\_\_ cudaError\_t cudaLaunchDevice(void \*kernel,

void \*params, dim3 gridDim,

dim3 blockDim,

unsigned int sharedMemSize = 0,

cudaStream\_t stream = 0);

### [C.3.1.8. API Reference](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "api-reference)

The portions of the CUDA Runtime API supported in the device runtime are detailed here. Host and device runtime APIs have identical syntax; semantics are the same except where indicated. The table below provides an overview of the API relative to the version available from the host.

| Table 5. Supported API Functions | |
| --- | --- |
| **Runtime API Functions** | **Details** |
| cudaDeviceSynchronize | Synchronizes on work launched from thread's own block only |
| cudaDeviceGetCacheConfig |  |
| cudaDeviceGetLimit |  |
| cudaGetLastError | Last error is per-thread state, not per-block state |
| cudaPeekAtLastError |  |
| cudaGetErrorString |  |
| cudaGetDeviceCount |  |
| cudaGetDeviceProperty | Will return properties for any device |
| cudaGetDevice | Always returns current device ID as would be seen from host |
| cudaStreamCreateWithFlags | Must pass cudaStreamNonBlocking flag |
| cudaStreamDestroy |  |
| cudaStreamWaitEvent |  |
| cudaEventCreateWithFlags | Must pass cudaEventDisableTiming flag |
| cudaEventRecord |  |
| cudaEventDestroy |  |
| cudaFuncGetAttributes |  |
| cudaMemcpyAsync | Notes about all memcpy/memset functions:   * Only async memcpy/set functions are supported * Only device-to-device memcpy is permitted * May not pass in local or shared memory pointers |
| cudaMemcpy2DAsync |
| cudaMemcpy3DAsync |
| cudaMemsetAsync |
| cudaMemset2DAsync |  |
| cudaMemset3DAsync |  |
| cudaRuntimeGetVersion |  |
| cudaMalloc | May not call cudaFree on the device on a pointer created on the host, and vice-versa |
| cudaFree |
| cudaOccupancyMaxActiveBlocksPerMultiprocessor |  |
| cudaOccupancyMaxPotentialBlockSize |  |
| cudaOccupancyMaxPotentialBlockSizeVariableSMem |  |

### [C.3.2. Device-side Launch from PTX](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "device-side-launch-from-ptx)

This section is for the programming language and compiler implementers who target Parallel Thread Execution (PTX) and plan to support Dynamic Parallelism in their language. It provides the low-level details related to supporting kernel launches at the PTX level.

### [C.3.2.1. Kernel Launch APIs](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "kernel-launch-apis)

Device-side kernel launches can be implemented using the following two APIs accessible from PTX: cudaLaunchDevice() and cudaGetParameterBuffer(). cudaLaunchDevice() launches the specified kernel with the parameter buffer that is obtained by calling cudaGetParameterBuffer() and filled with the parameters to the launched kernel. The parameter buffer can be NULL, i.e., no need to invoke cudaGetParameterBuffer(), if the launched kernel does not take any parameters.

### [C.3.2.1.1. cudaLaunchDevice](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "cudalaunchdevice)

At the PTX level, cudaLaunchDevice()needs to be declared in one of the two forms shown below before it is used.

// PTX-level Declaration of cudaLaunchDevice() when .address\_size is 64

.extern .func(.param .b32 func\_retval0) cudaLaunchDevice

(

.param .b64 func,

.param .b64 parameterBuffer,

.param .align 4 .b8 gridDimension[12],

.param .align 4 .b8 blockDimension[12],

.param .b32 sharedMemSize,

.param .b64 stream

)

;

// PTX-level Declaration of cudaLaunchDevice() when .address\_size is 32

.extern .func(.param .b32 func\_retval0) cudaLaunchDevice

(

.param .b32 func,

.param .b32 parameterBuffer,

.param .align 4 .b8 gridDimension[12],

.param .align 4 .b8 blockDimension[12],

.param .b32 sharedMemSize,

.param .b32 stream

)

;

The CUDA-level declaration below is mapped to one of the aforementioned PTX-level declarations and is found in the system header file cuda\_device\_runtime\_api.h. The function is defined in the cudadevrt system library, which must be linked with a program in order to use device-side kernel launch functionality.

// CUDA-level declaration of cudaLaunchDevice()

extern "C" \_\_device\_\_

cudaError\_t cudaLaunchDevice(void \*func, void \*parameterBuffer,

dim3 gridDimension, dim3 blockDimension,

unsigned int sharedMemSize,

cudaStream\_t stream);

The first parameter is a pointer to the kernel to be is launched, and the second parameter is the parameter buffer that holds the actual parameters to the launched kernel. The layout of the parameter buffer is explained in [Parameter Buffer Layout](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#parameter-buffer-layout), below. Other parameters specify the launch configuration, i.e., as grid dimension, block dimension, shared memory size, and the stream associated with the launch (please refer to [Execution Configuration](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#execution-configuration) for the detailed description of launch configuration.

### [C.3.2.1.2. cudaGetParameterBuffer](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "cudagetparameterbuffer)

cudaGetParameterBuffer() needs to be declared at the PTX level before it's used. The PTX-level declaration must be in one of the two forms given below, depending on address size:

// PTX-level Declaration of cudaGetParameterBuffer() when .address\_size is 64

// When .address\_size is 64

.extern .func(.param .b64 func\_retval0) cudaGetParameterBuffer

(

.param .b64 alignment,

.param .b64 size

)

;

// PTX-level Declaration of cudaGetParameterBuffer() when .address\_size is 32

.extern .func(.param .b32 func\_retval0) cudaGetParameterBuffer

(

.param .b32 alignment,

.param .b32 size

)

;

The following CUDA-level declaration of cudaGetParameterBuffer() is mapped to the aforementioned PTX-level declaration:

// CUDA-level Declaration of cudaGetParameterBuffer()

extern "C" \_\_device\_\_

void \*cudaGetParameterBuffer(size\_t alignment, size\_t size);

The first parameter specifies the alignment requirement of the parameter buffer and the second parameter the size requirement in bytes. In the current implementation, the parameter buffer returned by cudaGetParameterBuffer() is always guaranteed to be 64- byte aligned, and the alignment requirement parameter is ignored. However, it is recommended to pass the correct alignment requirement value - which is the largest alignment of any parameter to be placed in the parameter buffer - to cudaGetParameterBuffer() to ensure portability in the future.

### [C.3.2.2. Parameter Buffer Layout](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "parameter-buffer-layout)

Parameter reordering in the parameter buffer is prohibited, and each individual parameter placed in the parameter buffer is required to be aligned. That is, each parameter must be placed at the nth byte in the parameter buffer, where n is the smallest multiple of the parameter size that is greater than the offset of the last byte taken by the preceding parameter. The maximum size of the parameter buffer is 4KB.

For a more detailed description of PTX code generated by the CUDA compiler, please refer to the PTX-3.5 specification.

### [C.3.3. Toolkit Support for Dynamic Parallelism](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "toolkit-support-for-dynamic-parallelism)

### [C.3.3.1. Including Device Runtime API in CUDA Code](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "including-device-runtime-api-in-cuda-code)

Similar to the host-side runtime API, prototypes for the CUDA device runtime API are included automatically during program compilation. There is no need to include cuda\_device\_runtime\_api.h explicitly.

### [C.3.3.2. Compiling and Linking](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "compiling-and-linking)

CUDA programs are automatically linked with the host runtime library when compiled with nvcc, but the device runtime is shipped as a static library which must explicitly be linked with a program which wishes to use it.

The device runtime is offered as a static library (cudadevrt.lib on Windows, libcudadevrt.a under Linux and MacOS), against which a GPU application that uses the device runtime must be linked. Linking of device libraries can be accomplished through nvcc and/or nvlink. Two simple examples are shown below.

A device runtime program may be compiled and linked in a single step, if all required source files can be specified from the command line:

$ nvcc -arch=sm\_35 -rdc=true hello\_world.cu -o hello -lcudadevrt

It is also possible to compile CUDA .cu source files first to object files, and then link these together in a two-stage process:

$ nvcc -arch=sm\_35 -dc hello\_world.cu -o hello\_world.o

$ nvcc -arch=sm\_35 -rdc=true hello\_world.o -o hello -lcudadevrt

Please see the Using Separate Compilation section of The CUDA Driver Compiler NVCC guide for more details.

### [C.4. Programming Guidelines](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "programming-guidelines)

### [C.4.1. Basics](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "basics)

The device runtime is a functional subset of the host runtime. API level device management, kernel launching, device memcpy, stream management, and event management are exposed from the device runtime.

Programming for the device runtime should be familiar to someone who already has experience with CUDA. Device runtime syntax and semantics are largely the same as that of the host API, with any exceptions detailed earlier in this document.

The following example shows a simple Hello World program incorporating dynamic parallelism:

#include <stdio.h>

\_\_global\_\_ void childKernel()

{

printf("Hello ");

}

\_\_global\_\_ void parentKernel()

{

// launch child

childKernel<<<1,1>>>();

if (cudaSuccess != cudaGetLastError()) {

return;

}

// wait for child to complete

if (cudaSuccess != cudaDeviceSynchronize()) {

return;

}

printf("World!\n");

}

int main(int argc, char \*argv[])

{

// launch parent

parentKernel<<<1,1>>>();

if (cudaSuccess != cudaGetLastError()) {

return 1;

}

// wait for parent to complete

if (cudaSuccess != cudaDeviceSynchronize()) {

return 2;

}

return 0;

}

This program may be built in a single step from the command line as follows:

$ nvcc -arch=sm\_35 -rdc=true hello\_world.cu -o hello -lcudadevrt

### [C.4.2. Performance](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "performance)

### [C.4.2.1. Synchronization](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "synchronization-performance)

Synchronization by one thread may impact the performance of other threads in the same Thread Block, even when those other threads do not call cudaDeviceSynchronize() themselves. This impact will depend upon the underlying implementation.

### [C.4.2.2. Dynamic-parallelism-enabled Kernel Overhead](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "dynamic-parallelism-enabled-kernel-overhead)

System software which is active when controlling dynamic launches may impose an overhead on any kernel which is running at the time, whether or not it invokes kernel launches of its own. This overhead arises from the device runtime's execution tracking and management software and may result in decreased performance for e.g., library calls when made from the device compared to from the host side. This overhead is, in general, incurred for applications that link against the device runtime library.

### [C.4.3. Implementation Restrictions and Limitations](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "implementation-restrictions-and-limitations)

Dynamic Parallelism guarantees all semantics described in this document, however, certain hardware and software resources are implementation-dependent and limit the scale, performance and other properties of a program which uses the device runtime.

### [C.4.3.1. Runtime](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "runtime)

### [C.4.3.1.1. Memory Footprint](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "memory-footprint)

The device runtime system software reserves memory for various management purposes, in particular one reservation which is used for saving parent-grid state during synchronization, and a second reservation for tracking pending grid launches. Configuration controls are available to reduce the size of these reservations in exchange for certain launch limitations. See [Configuration Options](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#configuration-options), below, for details.

The majority of reserved memory is allocated as backing-store for parent kernel state, for use when synchronizing on a child launch. Conservatively, this memory must support storing of state for the maximum number of live threads possible on the device. This means that each parent generation at which cudaDeviceSynchronize() is callable may require up to 150MB of device memory, depending on the device configuration, which will be unavailable for program use even if it is not all consumed.

### [C.4.3.1.2. Nesting and Synchronization Depth](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "nesting-and-synchronization-depth)

Using the device runtime, one kernel may launch another kernel, and that kernel may launch another, and so on. Each subordinate launch is considered a new nesting level, and the total number of levels is the nesting depth of the program. The synchronization depth is defined as the deepest level at which the program will explicitly synchronize on a child launch. Typically this is one less than the nesting depth of the program, but if the program does not need to call cudaDeviceSynchronize() at all levels then the synchronization depth might be substantially different to the nesting depth.

The overall maximum nesting depth is limited to 24, but practically speaking the real limit will be the amount of memory required by the system for each new level (see [Memory Footprint](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#memory-footprint) above). Any launch which would result in a kernel at a deeper level than the maximum will fail. Note that this may also apply to cudaMemcpyAsync(), which might itself generate a kernel launch. See [Configuration Options](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#configuration-options) for details.

By default, sufficient storage is reserved for two levels of synchronization. This maximum synchronization depth (and hence reserved storage) may be controlled by calling cudaDeviceSetLimit() and specifying cudaLimitDevRuntimeSyncDepth. The number of levels to be supported must be configured before the top-level kernel is launched from the host, in order to guarantee successful execution of a nested program. Calling cudaDeviceSynchronize() at a depth greater than the specified maximum synchronization depth will return an error.

An optimization is permitted where the system detects that it need not reserve space for the parent's state in cases where the parent kernel never calls cudaDeviceSynchronize(). In this case, because explicit parent/child synchronization never occurs, the memory footprint required for a program will be much less than the conservative maximum. Such a program could specify a shallower maximum synchronization depth to avoid over-allocation of backing store.

### [C.4.3.1.3. Pending Kernel Launches](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "pending-kernel-launches)

When a kernel is launched, all associated configuration and parameter data is tracked until the kernel completes. This data is stored within a system-managed launch pool.

The launch pool is divided into a fixed-size pool and a virtualized pool with lower performance. The device runtime system software will try to track launch data in the fixed-size pool first. The virtualized pool will be used to track new launches when the fixed-size pool is full.

The size of the fixed-size launch pool is configurable by calling cudaDeviceSetLimit() from the host and specifying cudaLimitDevRuntimePendingLaunchCount.

### [C.4.3.1.4. Configuration Options](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "configuration-options)

Resource allocation for the device runtime system software is controlled via the cudaDeviceSetLimit() API from the host program. Limits must be set before any kernel is launched, and may not be changed while the GPU is actively running programs.

The following named limits may be set:

| **Limit** | **Behavior** |
| --- | --- |
| cudaLimitDevRuntimeSyncDepth | Sets the maximum depth at which cudaDeviceSynchronize() may be called. Launches may be performed deeper than this, but explicit synchronization deeper than this limit will return the cudaErrorLaunchMaxDepthExceeded. The default maximum sync depth is 2. |
| cudaLimitDevRuntimePendingLaunchCount | Controls the amount of memory set aside for buffering kernel launches which have not yet begun to execute, due either to unresolved dependencies or lack of execution resources. When the buffer is full, the device runtime system software will attempt to track new pending launches in a lower performance virtualized buffer. If the virtualized buffer is also full, i.e. when all available heap space is consumed, launches will not occur, and the thread's last error will be set to cudaErrorLaunchPendingCountExceeded. The default pending launch count is 2048 launches. |

### [C.4.3.1.5. Memory Allocation and Lifetime](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "memory-allocation-and-lifetime)

cudaMalloc() and cudaFree() have distinct semantics between the host and device environments. When invoked from the host, cudaMalloc() allocates a new region from unused device memory. When invoked from the device runtime these functions map to device-side malloc() and free(). This implies that within the device environment the total allocatable memory is limited to the device malloc() heap size, which may be smaller than the available unused device memory. Also, it is an error to invoke cudaFree() from the host program on a pointer which was allocated by cudaMalloc() on the device or vice-versa.

|  | **cudaMalloc() on Host** | **cudaMalloc() on Device** |
| --- | --- | --- |
| cudaFree() on Host | Supported | Not Supported |
| cudaFree() on Device | Not Supported | Supported |
| Allocation limit | Free device memory | cudaLimitMallocHeapSize |

### [C.4.3.1.6. SM Id and Warp Id](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "sm-id-and-warp-id)

Note that in PTX %smid and %warpid are defined as volatile values. The device runtime may reschedule thread blocks onto different SMs in order to more efficiently manage resources. As such, it is unsafe to rely upon %smid or %warpid remaining unchanged across the lifetime of a thread or thread block.

### [C.4.3.1.7. ECC Errors](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "ecc-errors)

No notification of ECC errors is available to code within a CUDA kernel. ECC errors are reported at the host side once the entire launch tree has completed. Any ECC errors which arise during execution of a nested program will either generate an exception or continue execution (depending upon error and configuration).

## [D. Mathematical Functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "mathematical-functions-appendix)

The reference manual lists, along with their description, all the functions of the C/C++ standard library mathematical functions that are supported in device code, as well as all intrinsic functions (that are only supported in device code).

This appendix provides accuracy information for some of these functions when applicable.

### [D.1. Standard Functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "standard-functions)

The functions from this section can be used in both host and device code.

This section specifies the error bounds of each function when executed on the device and also when executed on the host in the case where the host does not supply the function.

The error bounds are generated from extensive but not exhaustive tests, so they are not guaranteed bounds.

### Single-Precision Floating-Point Functions

Addition and multiplication are IEEE-compliant, so have a maximum error of 0.5 ulp.

The recommended way to round a single-precision floating-point operand to an integer, with the result being a single-precision floating-point number is rintf(), not roundf(). The reason is that roundf() maps to an 8-instruction sequence on the device, whereas rintf() maps to a single instruction. truncf(), ceilf(), and floorf() each map to a single instruction as well.

| Table 6. Single-Precision Mathematical Standard Library Functions with Maximum ULP Error. The maximum error is stated as the absolute value of the difference in ulps between a correctly rounded single-precision result and the result returned by the CUDA library function. | |
| --- | --- |
| **Function** | **Maximum ulp error** |
| x+y | 0 (IEEE-754 round-to-nearest-even) |
| x\*y | 0 (IEEE-754 round-to-nearest-even) |
| x/y | 0 for compute capability ≥ 2 when compiled with -prec-div=true  2 (full range), otherwise |
| 1/x | 0 for compute capability ≥ 2 when compiled with -prec-div=true  1 (full range), otherwise |
| rsqrtf(x)  1/sqrtf(x) | 2 (full range)  Applies to 1/sqrtf(x) only when it is converted to rsqrtf(x) by the compiler. |
| sqrtf(x) | 0 for compute capability ≥ 2 when compiled with -prec-sqrt=true  3 (full range), otherwise |
| cbrtf(x) | 1 (full range) |
| rcbrtf(x) | 1 (full range) |
| hypotf(x,y) | 3 (full range) |
| rhypotf(x,y) | 2 (full range) |
| norm3df(x,y,z) | 3 (full range) |
| rnorm3df(x,y,z) | 2 (full range) |
| norm4df(x,y,z,t) | 3 (full range) |
| expf(x) | 2 (full range) |
| exp2f(x) | 2 (full range) |
| exp10f(x) | 2 (full range) |
| expm1f(x) | 1 (full range) |
| logf(x) | 1 (full range) |
| log2f(x) | 2 (full range) |
| log10f(x) | 2 (full range) |
| log1pf(x) | 2 (full range) |
| sinf(x) | 2 (full range) |
| cosf(x) | 2 (full range) |
| tanf(x) | 4 (full range) |
| sincosf(x,sptr,cptr) | 2 (full range) |
| sinpif(x) | 2 (full range) |
| cospif(x) | 2 (full range) |
| sincospif(x,sptr,cptr) | 2 (full range) |
| asinf(x) | 4 (full range) |
| acosf(x) | 3 (full range) |
| atanf(x) | 2 (full range) |
| atan2f(y,x) | 3 (full range) |
| sinhf(x) | 3 (full range) |
| coshf(x) | 2 (full range) |
| tanhf(x) | 2 (full range) |
| asinhf(x) | 3 (full range) |
| acoshf(x) | 4 (full range) |
| atanhf(x) | 3 (full range) |
| powf(x,y) | 8 (full range) |
| erff(x) | 2 (full range) |
| erfcf(x) | 4 (full range) |
| erfinvf(x) | 2 (full range) |
| erfcinvf(x) | 2 (full range) |
| erfcxf(x) | 4 (full range) |
| normcdff(x) | 5 (full range) |
| normcdfinvf(x) | 5 (full range) |
| lgammaf(x) | 6 (outside interval -10.001 ... -2.264; larger inside) |
| tgammaf(x) | 11 (full range) |
| fmaf(x,y,z) | 0 (full range) |
| frexpf(x,exp) | 0 (full range) |
| ldexpf(x,exp) | 0 (full range) |
| scalbnf(x,n) | 0 (full range) |
| scalblnf(x,l) | 0 (full range) |
| logbf(x) | 0 (full range) |
| ilogbf(x) | 0 (full range) |
| j0f(x) | 9 for |x| < 8  otherwise, the maximum absolute error is 2.2 x 10-6 |
| j1f(x) | 9 for |x| < 8  otherwise, the maximum absolute error is 2.2 x 10-6 |
| jnf(x) | For n = 128, the maximum absolute error is 2.2 x 10-6 |
| y0f(x) | 9 for |x| < 8  otherwise, the maximum absolute error is 2.2 x 10-6 |
| y1f(x) | 9 for |x| < 8  otherwise, the maximum absolute error is 2.2 x 10-6 |
| ynf(x) | ceil(2 + 2.5n) for |x| < n  otherwise, the maximum absolute error is 2.2 x 10-6 |
| cyl\_bessel\_i0f(x) | 6 (full range) |
| cyl\_bessel\_i1f(x) | 6 (full range) |
| fmodf(x,y) | 0 (full range) |
| remainderf(x,y) | 0 (full range) |
| remquof(x,y,iptr) | 0 (full range) |
| modff(x,iptr) | 0 (full range) |
| fdimf(x,y) | 0 (full range) |
| truncf(x) | 0 (full range) |
| roundf(x) | 0 (full range) |
| rintf(x) | 0 (full range) |
| nearbyintf(x) | 0 (full range) |
| ceilf(x) | 0 (full range) |
| floorf(x) | 0 (full range) |
| lrintf(x) | 0 (full range) |
| lroundf(x) | 0 (full range) |
| llrintf(x) | 0 (full range) |
| llroundf(x) | 0 (full range) |

### Double-Precision Floating-Point Functions

The recommended way to round a double-precision floating-point operand to an integer, with the result being a double-precision floating-point number is rint(), not round(). The reason is that round() maps to an 8-instruction sequence on the device, whereas rint() maps to a single instruction. trunc(), ceil(), and floor() each map to a single instruction as well.

| Table 7. Double-Precision Mathematical Standard Library Functions with Maximum ULP Error. The maximum error is stated as the absolute value of the difference in ulps between a correctly rounded double-precision result and the result returned by the CUDA library function. | |
| --- | --- |
| **Function** | **Maximum ulp error** |
| x+y | 0 (IEEE-754 round-to-nearest-even) |
| x\*y | 0 (IEEE-754 round-to-nearest-even) |
| x/y | 0 (IEEE-754 round-to-nearest-even) |
| 1/x | 0 (IEEE-754 round-to-nearest-even) |
| sqrt(x) | 0 (IEEE-754 round-to-nearest-even) |
| rsqrt(x) | 1 (full range) |
| cbrt(x) | 1 (full range) |
| rcbrt(x) | 1 (full range) |
| hypot(x,y) | 2 (full range) |
| rhypot(x,y) | 1 (full range) |
| norm3d(x,y,z) | 2 (full range) |
| rnorm3d(x,y,z) | 1 (full range) |
| norm4d(x,y,z,t) | 2 (full range) |
| exp(x) | 1 (full range) |
| exp2(x) | 1 (full range) |
| exp10(x) | 1 (full range) |
| expm1(x) | 1 (full range) |
| log(x) | 1 (full range) |
| log2(x) | 1 (full range) |
| log10(x) | 1 (full range) |
| log1p(x) | 1 (full range) |
| sin(x) | 1 (full range) |
| cos(x) | 1 (full range) |
| tan(x) | 2 (full range) |
| sincos(x,sptr,cptr) | 1 (full range) |
| sinpi(x) | 1 (full range) |
| cospi(x) | 1 (full range) |
| sincospi(x,sptr,cptr) | 1 (full range) |
| asin(x) | 2 (full range) |
| acos(x) | 1 (full range) |
| atan(x) | 2 (full range) |
| atan2(y,x) | 2 (full range) |
| sinh(x) | 1 (full range) |
| cosh(x) | 1 (full range) |
| tanh(x) | 1 (full range) |
| asinh(x) | 2 (full range) |
| acosh(x) | 2 (full range) |
| atanh(x) | 2 (full range) |
| pow(x,y) | 2 (full range) |
| erf(x) | 2 (full range) |
| erfc(x) | 4 (full range) |
| erfinv(x) | 5 (full range) |
| erfcinv(x) | 6 (full range) |
| erfcx(x) | 3 (full range) |
| normcdf(x) | 5 (full range) |
| normcdfinv(x) | 7 (full range) |
| lgamma(x) | 4 (outside interval -11.0001 ... -2.2637; larger inside) |
| tgamma(x) | 8 (full range) |
| fma(x,y,z) | 0 (IEEE-754 round-to-nearest-even) |
| frexp(x,exp) | 0 (full range) |
| ldexp(x,exp) | 0 (full range) |
| scalbn(x,n) | 0 (full range) |
| scalbln(x,l) | 0 (full range) |
| logb(x) | 0 (full range) |
| ilogb(x) | 0 (full range) |
| j0(x) | 7 for |x| < 8  otherwise, the maximum absolute error is 5 x 10-12 |
| j1(x) | 7 for |x| < 8  otherwise, the maximum absolute error is 5 x 10-12 |
| jn(x) | For n = 128, the maximum absolute error is 5 x 10-12 |
| y0(x) | 7 for |x| < 8  otherwise, the maximum absolute error is 5 x 10-12 |
| y1(x) | 7 for |x| < 8  otherwise, the maximum absolute error is 5 x 10-12 |
| yn(x) | For |x| > 1.5n, the maximum absolute error is 5 x 10-12 |
| cyl\_bessel\_i0(x) | 6 (full range) |
| cyl\_bessel\_i1(x) | 6 (full range) |
| fmod(x,y) | 0 (full range) |
| remainder(x,y) | 0 (full range) |
| remquo(x,y,iptr) | 0 (full range) |
| mod(x,iptr) | 0 (full range) |
| fdim(x,y) | 0 (full range) |
| trunc(x) | 0 (full range) |
| round(x) | 0 (full range) |
| rint(x) | 0 (full range) |
| nearbyint(x) | 0 (full range) |
| ceil(x) | 0 (full range) |
| floor(x) | 0 (full range) |
| lrint(x) | 0 (full range) |
| lround(x) | 0 (full range) |
| llrint(x) | 0 (full range) |
| llround(x) | 0 (full range) |

### [D.2. Intrinsic Functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "intrinsic-functions)

The functions from this section can only be used in device code.

Among these functions are the less accurate, but faster versions of some of the functions of [Standard Functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#standard-functions) .They have the same name prefixed with \_\_ (such as \_\_sinf(x)). They are faster as they map to fewer native instructions. The compiler has an option (-use\_fast\_math) that forces each function in [Table 8](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#intrinsic-functions__functions-affected-use-fast-math) to compile to its intrinsic counterpart. In addition to reducing the accuracy of the affected functions, it may also cause some differences in special case handling. A more robust approach is to selectively replace mathematical function calls by calls to intrinsic functions only where it is merited by the performance gains and where changed properties such as reduced accuracy and different special case handling can be tolerated.

| Table 8. Functions Affected by -use\_fast\_math | |
| --- | --- |
| **Operator/Function** | **Device Function** |
| x/y | \_\_fdividef(x,y) |
| sinf(x) | \_\_sinf(x) |
| cosf(x) | \_\_cosf(x) |
| tanf(x) | \_\_tanf(x) |
| sincosf(x,sptr,cptr) | \_\_sincosf(x,sptr,cptr) |
| logf(x) | \_\_logf(x) |
| log2f(x) | \_\_log2f(x) |
| log10f(x) | \_\_log10f(x) |
| expf(x) | \_\_expf(x) |
| exp10f(x) | \_\_exp10f(x) |
| powf(x,y) | \_\_powf(x,y) |

Functions suffixed with \_rn operate using the round to nearest even rounding mode.

Functions suffixed with \_rz operate using the round towards zero rounding mode.

Functions suffixed with \_ru operate using the round up (to positive infinity) rounding mode.

Functions suffixed with \_rd operate using the round down (to negative infinity) rounding mode.

### Single-Precision Floating-Point Functions

\_\_fadd\_[rn,rz,ru,rd]() and \_\_fmul\_[rn,rz,ru,rd]() map to addition and multiplication operations that the compiler never merges into FMADs. By contrast, additions and multiplications generated from the '\*' and '+' operators will frequently be combined into FMADs.

The accuracy of floating-point division varies depending on whether the code is compiled with -prec-div=false or -prec-div=true. When the code is compiled with -prec-div=false, both the regular division / operator and \_\_fdividef(x,y) have the same accuracy, but for 2126 < y < 2128, \_\_fdividef(x,y) delivers a result of zero, whereas the / operator delivers the correct result to within the accuracy stated in [Table 9](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#intrinsic-functions__single-precision-floating-point-intrinsic-functions-supported-by-cuda-runtime-library). Also, for 2126 < y < 2128, if x is infinity, \_\_fdividef(x,y) delivers a NaN (as a result of multiplying infinity by zero), while the / operator returns infinity. On the other hand, the / operator is IEEE-compliant when the code is compiled with -prec-div=true or without any -prec-div option at all since its default value is true.

| Table 9. Single-Precision Floating-Point Intrinsic Functions. (Supported by the CUDA Runtime Library with Respective Error Bounds) | |
| --- | --- |
| **Function** | **Error bounds** |
| \_\_fadd\_[rn,rz,ru,rd](x,y) | IEEE-compliant. |
| \_\_fsub\_[rn,rz,ru,rd](x,y) | IEEE-compliant. |
| \_\_fmul\_[rn,rz,ru,rd](x,y) | IEEE-compliant. |
| \_\_fmaf\_[rn,rz,ru,rd](x,y,z) | IEEE-compliant. |
| \_\_frcp\_[rn,rz,ru,rd](x) | IEEE-compliant. |
| \_\_fsqrt\_[rn,rz,ru,rd](x) | IEEE-compliant. |
| \_\_frsqrt\_rn(x) | IEEE-compliant. |
| \_\_fdiv\_[rn,rz,ru,rd](x,y) | IEEE-compliant. |
| \_\_fdividef(x,y) | For y in [2-126, 2126], the maximum ulp error is 2. |
| \_\_expf(x) | The maximum ulp error is 2 + floor(abs(1.16 \* x)). |
| \_\_exp10f(x) | The maximum ulp error is 2+ floor(abs(2.95 \* x)). |
| \_\_logf(x) | For x in [0.5, 2], the maximum absolute error is 2-21.41, otherwise, the maximum ulp error is 3. |
| \_\_log2f(x) | For x in [0.5, 2], the maximum absolute error is 2-22, otherwise, the maximum ulp error is 2. |
| \_\_log10f(x) | For x in [0.5, 2], the maximum absolute error is 2-24, otherwise, the maximum ulp error is 3. |
| \_\_sinf(x) | For x in [-π,π], the maximum absolute error is 2-21.41, and larger otherwise. |
| \_\_cosf(x) | For x in [-π,π], the maximum absolute error is 2-21.19, and larger otherwise. |
| \_\_sincosf(x,sptr,cptr) | Same as \_\_sinf(x) and \_\_cosf(x). |
| \_\_tanf(x) | Derived from its implementation as \_\_sinf(x) \* (1/\_\_cosf(x)). |
| \_\_powf(x, y) | Derived from its implementation as exp2f(y \* \_\_log2f(x)). |

### Double-Precision Floating-Point Functions

\_\_dadd\_rn() and \_\_dmul\_rn() map to addition and multiplication operations that the compiler never merges into FMADs. By contrast, additions and multiplications generated from the '\*' and '+' operators will frequently be combined into FMADs.

| Table 10. Double-Precision Floating-Point Intrinsic Functions. (Supported by the CUDA Runtime Library with Respective Error Bounds) | |
| --- | --- |
| **Function** | **Error bounds** |
| \_\_dadd\_[rn,rz,ru,rd](x,y) | IEEE-compliant. |
| \_\_dsub\_[rn,rz,ru,rd](x,y) | IEEE-compliant. |
| \_\_dmul\_[rn,rz,ru,rd](x,y) | IEEE-compliant. |
| \_\_fma\_[rn,rz,ru,rd](x,y,z) | IEEE-compliant. |
| \_\_ddiv\_[rn,rz,ru,rd](x,y)(x,y) | IEEE-compliant.  Requires compute capability > 2. |
| \_\_drcp\_[rn,rz,ru,rd](x) | IEEE-compliant.  Requires compute capability > 2. |
| \_\_dsqrt\_[rn,rz,ru,rd](x) | IEEE-compliant.  Requires compute capability > 2. |

## [E. C/C++ Language Support](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "c-cplusplus-language-support)

As described in [Compilation with NVCC](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compilation-with-nvcc), source files compiled with nvcc can include a mix of host code and device code.

For the host code, nvcc supports whatever part of the C++ ISO/IEC 14882:2003 specification the host c++ compiler supports.

For the device code, nvcc supports the features illustrated in [Code Samples](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#code-samples) with some restrictions described in [Restrictions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#restrictions); it does not support run time type information (RTTI), exception handling, and the C++ Standard Library.

### [E.1. Code Samples](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "code-samples)

### [E.1.1. Data Aggregation Class](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "data-aggregation-class)

class PixelRGBA {

public:

\_\_device\_\_ PixelRGBA(): r\_(0), g\_(0), b\_(0), a\_(0) { }

\_\_device\_\_ PixelRGBA(unsigned char r, unsigned char g,

unsigned char b, unsigned char a = 255):

r\_(r), g\_(g), b\_(b), a\_(a) { }

private:

unsigned char r\_, g\_, b\_, a\_;

friend PixelRGBA operator+(const PixelRGBA const PixelRGBA&);

};

\_\_device\_\_

PixelRGBA operator+(const PixelRGBA& p1, const PixelRGBA& p2)

{

return PixelRGBA(p1.r\_ + p2.r\_, p1.g\_ + p2.g\_,

p1.b\_ + p2.b\_, p1.a\_ + p2.a\_);

}

\_\_device\_\_ void func(void)

{

PixelRGBA p1, p2;

// ... // Initialization of p1 and p2 here

PixelRGBA p3 = p1 + p2;

}

### [E.1.2. Derived Class](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "derived-class)

\_\_device\_\_ void\* operator new(size\_t bytes, MemoryPool& p);

\_\_device\_\_ void operator delete(void\*, MemoryPool& p);

class Shape {

public:

\_\_device\_\_ Shape(void) { }

\_\_device\_\_ void putThis(PrintBuffer \*p) const;

\_\_device\_\_ virtual void Draw(PrintBuffer \*p) const {

p->put("Shapeless");

}

\_\_device\_\_ virtual ~Shape() {}

};

class Point : public Shape {

public:

\_\_device\_\_ Point() : x(0), y(0) {}

\_\_device\_\_ Point(int ix, int iy) : x(ix), y(iy) { }

\_\_device\_\_ void PutCoord(PrintBuffer \*p) const;

\_\_device\_\_ void Draw(PrintBuffer \*p) const;

\_\_device\_\_ ~Point() {}

private:

int x, y;

};

\_\_device\_\_ Shape\* GetPointObj(MemoryPool& pool)

{

Shape\* shape = new(pool) Point(rand(-20,10), rand(-100,-20));

return shape;

}

### [E.1.3. Class Template](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "class-template)

template <class T>

class myValues {

T values[MAX\_VALUES];

public:

\_\_device\_\_ myValues(T clear) { ... }

\_\_device\_\_ void setValue(int Idx, T value) { ... }

\_\_device\_\_ void putToMemory(T\* valueLocation) { ... }

};

template <class T>

void \_\_global\_\_ useValues(T\* memoryBuffer) {

myValues<T> myLocation(0);

...

}

\_\_device\_\_ void\* buffer;

int main()

{

...

useValues<int><<<blocks, threads>>>(buffer);

...

}

### [E.1.4. Function Template](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "function-template)

template <typename T>

\_\_device\_\_ bool func(T x)

{

...

return (...);

}

template <>

\_\_device\_\_ bool func<int>(T x) // Specialization

{

return true;

}

// Explicit argument specification

bool result = func<double>(0.5);

// Implicit argument deduction

int x = 1;

bool result = func(x);

### [E.1.5. Functor Class](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "functor-class)

class Add {

public:

\_\_device\_\_ float operator() (float a, float b) const

{

return a + b;

}

};

class Sub {

public:

\_\_device\_\_ float operator() (float a, float b) const

{

return a - b;

}

};

// Device code

template<class O> \_\_global\_\_

void VectorOperation(const float \* A, const float \* B, float \* C,

unsigned int N, O op)

{

unsigned int iElement = blockDim.x \* blockIdx.x + threadIdx.x;

if (iElement < N)

C[iElement] = op(A[iElement], B[iElement]);

}

// Host code

int main()

{

...

VectorOperation<<<blocks, threads>>>(v1, v2, v3, N, Add());

...

}

### [E.2. Restrictions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "restrictions)

### [E.2.1. Preprocessor Symbols](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "preprocessor-symbols)

### [E.2.1.1. \_\_CUDA\_ARCH\_\_](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "cuda-arch-macro)

1. The type signature of the following entities shall not depend on whether \_\_CUDA\_ARCH\_\_ is defined or not, or on a particular value of \_\_CUDA\_ARCH\_\_:
   * \_\_global\_\_ functions and function templates
   * \_\_device\_\_ and \_\_constant\_\_ variables
   * textures and surfaces

Example:

#if !defined(\_\_CUDA\_ARCH\_\_)

typedef int mytype;

#else

typedef double mytype;

#endif

\_\_device\_\_ mytype xxx; // error: xxx's type depends on \_\_CUDA\_ARCH\_\_

\_\_global\_\_ void foo(mytype in, // error: foo's type depends on \_\_CUDA\_ARCH\_\_

mytype \*ptr)

{

\*ptr = in;

}

1. If a \_\_global\_\_ function template is instantiated and launched from the host, then the function template must be instantiated with the same template arguments irrespective of whether \_\_CUDA\_ARCH\_\_ is defined and regardless of the value of \_\_CUDA\_ARCH\_\_.

Example:

\_\_device\_\_ int result;

template <typename T>

\_\_global\_\_ void kern(T in)

{

result = in;

}

\_\_host\_\_ \_\_device\_\_ void foo(void)

{

#if !defined(\_\_CUDA\_ARCH\_\_)

kern<<<1,1>>>(1); // error: "kern<int>" instantiation only

// when \_\_CUDA\_ARCH\_\_ is undefined!

#endif

}

int main(void)

{

foo();

cudaDeviceSynchronize();

return 0;

}

1. In separate compilation mode, the presence or absence of a definition of a function or variable with external linkage shall not depend on whether \_\_CUDA\_ARCH\_\_ is defined or on a particular value of \_\_CUDA\_ARCH\_\_[7](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "fntarg_7).

Example:

#if !defined(\_\_CUDA\_ARCH\_\_)

void foo(void) { } // error: The definition of foo()

// is only present when \_\_CUDA\_ARCH\_\_

// is undefined

#endif

1. In separate compilation, \_\_CUDA\_ARCH\_\_ must not be used in headers such that different objects could contain different behavior. Or, it must be guaranteed that all objects will compile for the same compute\_arch. If a weak function or template function is defined in a header and its behavior depends on \_\_CUDA\_ARCH\_\_, then the instances of that function in the objects could conflict if the objects are compiled for different compute arch.

For example, if an a.h contains:

template<typename T>

\_\_device\_\_ T\* getptr(void)

{

#if \_\_CUDA\_ARCH\_\_ == 200

return NULL; /\* no address \*/

#else

\_\_shared\_\_ T arr[256];

return arr;

#endif

}

Then if a.cu and b.cu both include a.h and instantiate getptr for the same type, and b.cu expects a non-NULL address, and compile with:

nvcc –arch=compute\_20 –dc a.cu

nvcc –arch=compute\_30 –dc b.cu

nvcc –arch=sm\_30 a.o b.o

At link time only one version of the getptr is used, so the behavior would depend on which version is picked. To avoid this, either a.cu and b.cu must be compiled for the same compute arch, or \_\_CUDA\_ARCH\_\_ should not be used in the shared header function.

The compiler does not guarantee that a diagnostic will be generated for the unsupported uses of \_\_CUDA\_ARCH\_\_ described above.

### [E.2.2. Qualifiers](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "qualifiers)

### [E.2.2.1. Device Memory Qualifiers](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "device-memory-qualifiers)

The \_\_device\_\_, \_\_shared\_\_ and \_\_constant\_\_ qualifiers are not allowed on:

* class, struct, and union data members,
* formal parameters,
* local variables within a function that executes on the host.

\_\_shared\_\_ and \_\_constant\_\_ variables have implied static storage.

\_\_device\_\_ and \_\_constant\_\_ variable definitions are only allowed in namespace scope (including global namespace scope).

\_\_device\_\_, \_\_constant\_\_ and \_\_shared\_\_ variables defined in namespace scope, that are of class type, cannot have a non-empty constructor or a non-empty destructor. A constructor for a class type is considered empty at a point in the translation unit, if it is either a trivial constructor or it satisfies all of the following conditions:

* The constructor function has been defined.
* The constructor function has no parameters, the initializer list is empty and the function body is an empty compound statement.
* Its class has no virtual functions and no virtual base classes.
* The default constructors of all base classes of its class can be considered empty.
* For all the nonstatic data members of its class that are of class type (or array thereof), the default constructors can be considered empty.

A destructor for a class is considered empty at a point in the translation unit, if it is either a trivial destructor or it satisfies all of the following conditions:

* The destructor function has been defined.
* The destructor function body is an empty compound statement.
* Its class has no virtual functions and no virtual base classes.
* The destructors of all base classes of its class can be considered empty.
* For all the nonstatic data members of its class that are of class type (or array thereof), the destructor can be considered empty.

When compiling in the whole program compilation mode (see the nvcc user manual for a description of this mode), \_\_device\_\_, \_\_shared\_\_, and \_\_constant\_\_ variables cannot be defined as external using the extern keyword. The only exception is for dynamically allocated \_\_shared\_\_ variables as described in [\_\_shared\_\_](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#shared).

When compiling in the separate compilation mode (see the nvcc user manual for a description of this mode), \_\_device\_\_, \_\_shared\_\_, and \_\_constant\_\_ variables can be defined as external using the extern keyword. nvlink will generate an error when it cannot find a definition for an external variable (unless it is a dynamically allocated \_\_shared\_\_ variable).

### [E.2.2.2. \_\_managed\_\_ Qualifier](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "managed-qualifier)

Variables marked with the \_\_managed\_\_ qualifier ("managed" variables) have the following restrictions:

* The address of a managed variable is not a constant expression.
* A managed variable shall not have a const qualified type.
* A managed variable shall not have a reference type.
* The address or value of a managed variable shall not be used when the CUDA runtime may not be in a valid state, including the following cases:
  + In static/dynamic initialization or destruction of an object with static or thread local storage duration.
  + In code that executes after exit() has been called (e.g., a function marked with gcc's "\_\_attribute\_\_((destructor))").
  + In code that executes when CUDA runtime may not be initialized (e.g., a function marked with gcc's "\_\_attribute\_\_((constructor))").
* A managed variable cannot be used as an unparenthesized id-expression argument to a decltype() expression.
* Managed variables have the same coherence and consistency behavior as specified for dynamically allocated managed memory.
* When a CUDA program containing managed variables is run on an execution platform with multiple GPUs, the variables are allocated only once, and not per GPU.

Here are examples of legal and illegal uses of managed variables:

\_\_device\_\_ \_\_managed\_\_ int xxx = 10; // OK

int \*ptr = &xxx; // error: use of managed variable

// (xxx) in static initialization

struct S1\_t {

int field;

S1\_t(void) : field(xxx) { };

};

struct S2\_t {

~S2\_t(void) { xxx = 10; }

};

S1\_t temp1; // error: use of managed variable

// (xxx) in dynamic initialization

S2\_t temp2; // error: use of managed variable

// (xxx) in the destructor of

// object with static storage

// duration

\_\_device\_\_ \_\_managed\_\_ const int yyy = 10; // error: const qualified type

\_\_device\_\_ \_\_managed\_\_ int &zzz = xxx; // error: reference type

template <int \*addr> struct S3\_t { };

S3\_t<&xxx> temp; // error: address of managed

// variable(xxx) not a

// constant expression

\_\_global\_\_ void kern(int \*ptr)

{

assert(ptr == &xxx); // OK

xxx = 20; // OK

}

int main(void)

{

int \*ptr = &xxx; // OK

kern<<<1,1>>>(ptr);

cudaDeviceSynchronize();

xxx++; // OK

decltype(xxx) qqq; // error: managed variable(xxx) used

// as unparenthized argument to

// decltype

decltype((xxx)) zzz = yyy; // OK

}

### [E.2.2.3. Volatile Qualifier](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "volatile-qualifier)

The compiler is free to optimize reads and writes to global or shared memory (for example, by caching global reads into registers or L1 cache) as long as it respects the memory ordering semantics of memory fence functions ([Memory Fence Functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#memory-fence-functions)) and memory visibility semantics of synchronization functions ([Synchronization Functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#synchronization-functions)).

These optimizations can be disabled using the volatile keyword: If a variable located in global or shared memory is declared as volatile, the compiler assumes that its value can be changed or used at any time by another thread and therefore any reference to this variable compiles to an actual memory read or write instruction.

### [E.2.3. Pointers](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "pointers)

Dereferencing a pointer either to global or shared memory in code that is executed on the host, or to host memory in code that is executed on the device results in an undefined behavior, most often in a segmentation fault and application termination.

The address obtained by taking the address of a \_\_device\_\_, \_\_shared\_\_ or \_\_constant\_\_ variable can only be used in device code. The address of a \_\_device\_\_ or \_\_constant\_\_ variable obtained through cudaGetSymbolAddress() as described in [Device Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#device-memory) can only be used in host code.

As a consequence of the use of C++ syntax rules, void pointers (e.g., returned by malloc()) cannot be assigned to non-void pointers without a typecast.

### [E.2.4. Operators](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "operators)

### [E.2.4.1. Assignment Operator](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "assignment-operator)

\_\_constant\_\_ variables can only be assigned from the host code through runtime functions ([Device Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#device-memory)); they cannot be assigned from the device code.

\_\_shared\_\_ variables cannot have an initialization as part of their declaration.

It is not allowed to assign values to any of the built-in variables defined in [Built-in Variables](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#built-in-variables).

### [E.2.4.2. Address Operator](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "address-operator)

It is not allowed to take the address of any of the built-in variables defined in [Built-in Variables](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#built-in-variables).

### [E.2.5. Functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "functions)

### [E.2.5.1. External Linkage](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "external-linkage)

A call within some device code of a function declared with the extern qualifier is only allowed if the function is defined within the same compilation unit as the device code, i.e., a single file or several files linked together with relocatable device code and nvlink.

### [E.2.5.2. Compiler generated functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "compiler-generated-functions)

The execution space qualifiers (\_\_host\_\_, \_\_device\_\_) for a compiler generated function are the union of the execution space qualifiers of all the functions that invoke it (note that a \_\_global\_\_ caller will be treated as a \_\_device\_\_ caller for this analysis). For example:

class Base {

int x;

public:

\_\_host\_\_ \_\_device\_\_ Base(void) : x(10) {}

};

class Derived : public Base {

int y;

};

class Other: public Base {

int z;

};

\_\_device\_\_ void foo(void)

{

Derived D1;

Other D2;

}

\_\_host\_\_ void bar(void)

{

Other D3;

}

Here, the compiler generated constructor function "Derived::Derived" will be treated as a \_\_device\_\_ function, since it is invoked only from the \_\_device\_\_ function "foo". The compiler generated constructor function "Other::Other" will be treated as a \_\_host\_\_ \_\_device\_\_ function, since it is invoked both from a \_\_device\_\_ function "foo" and a \_\_host\_\_ function "bar".

### [E.2.5.3. Function Parameters](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "function-parameters)

\_\_global\_\_ function parameters are passed to the device via constant memory and are limited to 4 KB.

\_\_device\_\_ and \_\_global\_\_ functions cannot have a variable number of arguments.

### [E.2.5.4. Static Variables within Function](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "static-variables-function)

Within the body of a \_\_device\_\_ or \_\_global\_\_ function, only \_\_shared\_\_ variables may be declared with static storage class.

### [E.2.5.5. Function Pointers](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "function-pointers)

The address of a \_\_global\_\_ function taken in host code cannot be used in device code (e.g. to launch the kernel). Similarly, the address of a \_\_global\_\_ function taken in device code [8](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "fntarg_8) cannot be used in host code.

It is not allowed to take the address of a \_\_device\_\_ function in host code.

### [E.2.5.6. Function Recursion](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "function-recursion)

\_\_global\_\_ functions do not support recursion.

### [E.2.6. Classes](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "classes)

### [E.2.6.1. Data Members](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "data-members)

Static data members are not supported.

The layout of bit-fields in device code may currently not match the layout in host code on Windows.

### [E.2.6.2. Function Members](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "function-members)

Static member functions cannot be \_\_global\_\_ functions.

### [E.2.6.3. Virtual Functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "virtual-functions)

When a function in a derived class overrides a virtual function in a base class, the execution space qualifiers (i.e., \_\_host\_\_, \_\_device\_\_) on the overridden and overriding functions must match.

It is not allowed to pass as an argument to a \_\_global\_\_ function an object of a class with virtual functions.

The virtual function table is placed in global or constant memory by the compiler.

### [E.2.6.4. Virtual Base Classes](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "virtual-base-classes)

It is not allowed to pass as an argument to a \_\_global\_\_ function an object of a class derived from virtual base classes.

### [E.2.6.5. Anonymous Unions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "anon-union)

Member variables of a namespace scope anonymous union cannot be referenced in a \_\_global\_\_ or \_\_device\_\_ function.

### [E.2.6.6. Windows-Specific](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "windows-specific)

On Windows, the CUDA compiler may produce a different memory layout, compared to the host Microsoft compiler, for a C++ object of class type T that satisfies any of the following conditions:

* T has virtual functions or derives from a direct or indirect base class that has virtual functions;
* T has a direct or indirect virtual base class;
* T has multiple inheritance with more than one direct or indirect empty base class.

The size for such an object may also be different in host and device code. As long as type T is used exclusively in host or device code, the program should work correctly. Do not pass objects of type T between host and device code (e.g., as arguments to \_\_global\_\_ functions or through cudaMemcpy\*() calls).

### [E.2.7. Templates](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "templates)

A type or template cannot be used in the type, non-type or template template argument of a \_\_global\_\_ function template instantiation if either:

* The type or template is defined within a \_\_host\_\_ or \_\_host\_\_ \_\_device\_\_.
* The type or template is a class member with private or protected access and its parent class is not defined within a \_\_device\_\_ or \_\_global\_\_ function.

Example:

template <typename T>

\_\_global\_\_ void myKernel(void) { }

class myClass {

private:

struct inner\_t { };

public:

static void launch(void)

{

// error: inner\_t is used in template argument

// but it is private

myKernel<inner\_t><<<1,1>>>();

}

};

### [E.2.8. Const-qualified variables](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "const-variables)

Let 'V' denote a namespace scope variable or a class static member variable that has const qualified type and does not have execution space annotations (e.g., \_\_device\_\_, \_\_constant\_\_, \_\_shared\_\_). V is considered to be a host code variable.

The value of V may be directly used in device code, if V has builtin floating point or integral type, and it has been initialized with a constant expression before the point of use. Device source code cannot contain a reference to V or take the address of V.

Example:

const int xxx = 10;

struct S1\_t { static const int yyy = 20; };

extern const int zzz;

\_\_device\_\_ void foo(void) {

int local1[xxx]; // OK

int local2[S1\_t::yyy]; // OK

int val1 = xxx; // OK

int val2 = S1\_t::yyy; // OK

int val3 = zzz; // error: zzz not initialized with constant

// expression at the point of use.

const int &val3 = xxx; // error: reference to host variable

const int \*val4 = &xxx; // error: address of host variable

}

const int zzz = 20;

### [E.2.9. C++11 Features](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "cpp11)

C++11 features that are enabled by default by the host compiler are also supported by nvcc, subject to the restrictions described in this document. In addition, invoking nvcc with -std=c++11 flag turns on all C++11 features and also invokes the host preprocessor, compiler and linker with the corresponding C++11 dialect option [9](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "fntarg_9).

### [E.2.9.1. Lambda Expressions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "lambda-expressions)

The execution space qualifiers for all member functions[10](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "fntarg_10) of the closure class associated with a lambda expression are derived by the compiler as follows. As described in the C++11 standard, the compiler creates a closure type in the smallest block scope, class scope or namespace scope that contains the lambda expression. The innermost function scope enclosing the closure type is computed, and the corresponding function's execution space qualifiers are assigned to the closure class member functions. If there is no enclosing function scope, the execution space qualifier is \_\_host\_\_.

Examples of lambda expressions and computed execution space qualifiers are shown below (in comments).

auto globalVar = [] { return 0; }; // \_\_host\_\_

void f1(void) {

auto l1 = [] { return 1; }; // \_\_host\_\_

}

\_\_device\_\_ void f2(void) {

auto l2 = [] { return 2; }; // \_\_device\_\_

}

\_\_host\_\_ \_\_device\_\_ void f3(void) {

auto l3 = [] { return 3; }; // \_\_host\_\_ \_\_device\_\_

}

\_\_device\_\_ void f4(int (\*fp)() = [] { return 4; } /\* \_\_host\_\_ \*/) {

}

\_\_global\_\_ void f5(void) {

auto l5 = [] { return 5; }; // \_\_device\_\_

}

\_\_device\_\_ void f6(void) {

struct S1\_t {

static void helper(int (\*fp)() = [] {return 6; } /\* \_\_device\_\_ \*/) {

}

};

}

The closure type of a lambda expression cannot be used in the type or non-type argument of a \_\_global\_\_ function template instantiation, unless the lambda is defined within a \_\_device\_\_ or \_\_global\_\_ function.

Example:

template <typename T>

\_\_global\_\_ void foo(T in) { };

template <typename T>

struct S1\_t { };

void bar(void) {

auto temp1 = [] { };

foo<<<1,1>>>(temp1); // error: lambda closure type used in

// template type argument

foo<<<1,1>>>( S1\_t<decltype(temp1)>()); // error: lambda closure type used in

// template type argument

}

### [E.2.9.2. std::initializer\_list](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "initializer-list)

By default, the CUDA compiler will implicitly consider the member functions of std::initializer\_list to have \_\_host\_\_ \_\_device\_\_ execution space qualifiers, and therefore they can be invoked directly from device code. The nvcc flag --no-host-device-initializer-list will disable this behavior; member functions of std::initializer\_list will then be considered as \_\_host\_\_ functions and will not be directly invokable from device code.

Example:

#include <initializer\_list>

\_\_device\_\_ int foo(std::initializer\_list<int> in);

\_\_device\_\_ void bar(void)

{

foo({4,5,6}); // (a) initializer list containing only

// constant expressions.

int i = 4;

foo({i,5,6}); // (b) initializer list with at least one

// non-constant element.

// This form may have better performance than (a).

}

### [E.2.9.3. Rvalue references](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "rvalue-references)

By default, the CUDA compiler will implicitly consider std::move and std::forward function templates to have \_\_host\_\_ \_\_device\_\_ execution space qualifiers, and therefore they can be invoked directly from device code. The nvcc flag --no-host-device-move-forward will disable this behavior; std::move and std::forward will then be considered as \_\_host\_\_ functions and will not be directly invokable from device code.

### [E.2.9.4. Constexpr functions and function templates](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "constexpr-functions)

By default, a constexpr function cannot be called from a function with incompatible execution space [11](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "fntarg_11). The experimental nvcc flag --relaxed-constexpr removes this restriction. When this flag is specified, host code can invoke a \_\_device\_\_ constexpr function and device code can invoke a \_\_host\_\_ constexpr function. Note that a function template instantiation may not be a constexpr function even if the corresponding template is marked with the keyword constexpr (C++11 Standard Section [dcl.constexpr.p6]).

### [E.2.9.5. Constexpr variables](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "constexpr-variables)

Let 'V' denote a namespace scope variable or a class static member variable that has been marked constexpr and that does not have execution space annotations (e.g., \_\_device\_\_, \_\_constant\_\_, \_\_shared\_\_). V is considered to be a host code variable.

The value of V can be used directly in device code. Device source code cannot contain a reference to V or take the address of V.

Example:

constexpr int xxx = 10;

constexpr int yyy = xxx + 4;

struct S1\_t { static constexpr int qqq = 100; };

\_\_device\_\_ int foo(void) {

int v1 = xxx + yyy + S1\_t::qqq; // OK

const int &v2 = xxx; // error: reference to host constexpr

// variable

const int \*v3 = &xxx; // error: address of host constexpr

// variable

const int &v4 = S1\_t::qqq; // error: reference to host constexpr

// variable

const int \*v5 = &S1\_t::qqq; // error: address of host constexpr

// variable

return v1;

}

### [E.2.9.6. Inline namespaces](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "inline-namespaces)

For an input CUDA translation unit, the CUDA compiler may invoke the host compiler for compiling the host code within the translation unit. In the code passed to the host compiler, the CUDA compiler will inject additional compiler generated code, if the input CUDA translation unit contained a definition of any of the following entities:

* \_\_global\_\_ function or function template instantiation
* \_\_device\_\_, \_\_constant\_\_
* variables with surface or texture type

The compiler generated code contains a reference to the defined entity. If the entity is defined within an inline namespace and another entity of the same name and type signature is defined in an enclosing namespace, this reference may be considered ambiguous by the host compiler and host compilation will fail.

This limitation can be avoided by using unique names for such entities defined within an inline namespace.

Example:

\_\_device\_\_ int Gvar;

inline namespace N1 {

\_\_device\_\_ int Gvar;

}

// <-- CUDA compiler inserts a reference to "Gvar" at this point in the

// translation unit. This reference will be considered ambiguous by the

// host compiler and compilation will fail.

}

Example:

inline namespace N1 {

namespace N2 {

\_\_device\_\_ int Gvar;

}

}

namespace N2 {

\_\_device\_\_ int Gvar;

}

// <-- CUDA compiler inserts reference to "::N2::Gvar" at this point in

// the translation unit. This reference will be considered ambiguous by

// the host compiler and compilation will fail.

}

### [E.2.9.6.1. Inline unnamed namespaces](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "inline-unnamed-namespaces)

The following entities cannot be declared in namespace scope within an inline unnamed namespace:

* \_\_device\_\_, \_\_shared\_\_ and \_\_constant\_\_ variables
* \_\_global\_\_ function and function templates
* variables with surface or texture type

Example:

inline namespace {

namespace N2 {

template <typename T>

\_\_global\_\_ void foo(void); // error

\_\_global\_\_ void bar(void) { } // error

template <>

\_\_global\_\_ void foo<int>(void) { } // error

\_\_device\_\_ int x1b; // error

\_\_constant\_\_ int x2b; // error

\_\_shared\_\_ int x3b; // error

texture<int> q2; // error

surface<int> s2; // error

}

};

### [E.2.9.7. thread\_local](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "thread-local)

The thread\_local storage specifier is not allowed in device code.

### [E.2.9.8. \_\_global\_\_ functions and function templates](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "cpp11-global)

A \_\_global\_\_ function or function template cannot be declared as constexpr and cannot have trailing return type.

The following types are not allowed for a parameter of a \_\_global\_\_ function or function template:

* rvalue reference type
* std::initializer\_list
* restrict qualified reference type

A variadic \_\_global\_\_ function template has the following restrictions:

* Only a single pack parameter is allowed.
* The pack parameter must be listed last in the template parameter list.

Example:

// ok

template <template <typename...> class Wrapper, typename... Pack>

\_\_global\_\_ void foo1(Wrapper<Pack...>);

// error: pack parameter is not last in parameter list

template <typename... Pack, template <typename...> class Wrapper>

\_\_global\_\_ void foo2(Wrapper<Pack...>);

// error: multiple parameter packs

template <typename... Pack1, int...Pack2, template<typename...> class Wrapper1,

template<int...> class Wrapper2>

\_\_global\_\_ void foo3(Wrapper1<Pack1...>, Wrapper2<Pack2...>);

### [E.2.9.9. \_\_device\_\_/\_\_constant\_\_/\_\_shared\_\_ variables](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "cpp11-device-variable)

\_\_device\_\_, \_\_constant\_\_ and \_\_shared\_\_ variables cannot be marked with the keyword constexpr and cannot have rvalue reference type.

### [E.3. Polymorphic Function Wrappers](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "polymorphic-function-wrappers)

A polymorphic function wrapper class template nvstd::function is provided in the nvfunctional header. Instances of this class template can be used to store, copy and invoke any callable target, e.g., lambda expressions. The operator() for instances of nvstd::function is a \_\_device\_\_ function, and can therefore be invoked only from device code.

Example:

#include <nvfunctional>

\_\_device\_\_ void foo() { }

\_\_global\_\_ void k() {

/\* Assign address of \_\_device\_\_ function \*/

nvstd::function<void()> fn1 = foo;

fn1(); /\* invoke \*/

auto lambda = [](int) { return 10.1f; };

/\* Assign lambda closure object \*/

nvstd::function<float (int)> fn2 = lambda;

fn2(10); /\* invoke \*/

}

\_\_host\_\_ void bar1(nvstd::function<void()> in) {

in(); /\* error: invoking device function from host code \*/

}

\_\_host\_\_ \_\_device\_\_ void bar2(nvstd::function<void()> in) {

in(); /\* error: invoking device function from host code \*/

#ifdef \_\_CUDA\_ARCH\_\_

in(); /\* ok \*/

#endif /\* \_\_CUDA\_ARCH\_\_ \*/

}

nvstd::function is defined in the nvfunctional header as follows:

namespace nvstd {

template <class \_RetType, class ...\_ArgTypes>

class function<\_RetType(\_ArgTypes...)>

{

public:

// constructors

\_\_device\_\_ \_\_host\_\_ function() noexcept;

\_\_device\_\_ \_\_host\_\_ function(nullptr\_t) noexcept;

\_\_device\_\_ \_\_host\_\_ function(const function &);

\_\_device\_\_ \_\_host\_\_ function(function &&);

template<class \_F>

\_\_device\_\_ \_\_host\_\_ function(\_F);

// destructor

\_\_device\_\_ \_\_host\_\_ ~function();

// assignment operators

\_\_device\_\_ \_\_host\_\_ function& operator=(const function&);

\_\_device\_\_ \_\_host\_\_ function& operator=(function&&);

\_\_device\_\_ \_\_host\_\_ function& operator=(nullptr\_t);

\_\_device\_\_ \_\_host\_\_ function& operator=(\_F&&);

// swap

\_\_device\_\_ \_\_host\_\_ void swap(function&) noexcept;

// function capacity

\_\_device\_\_ \_\_host\_\_ explicit operator bool() const noexcept;

// function invocation

\_\_device\_\_ \_RetType operator()(\_ArgTypes...) const;

};

// null pointer comparisons

template <class \_R, class... \_ArgTypes>

\_\_device\_\_ \_\_host\_\_

bool operator==(const function<\_R(\_ArgTypes...)>&, nullptr\_t) noexcept;

template <class \_R, class... \_ArgTypes>

\_\_device\_\_ \_\_host\_\_

bool operator==(nullptr\_t, const function<\_R(\_ArgTypes...)>&) noexcept;

template <class \_R, class... \_ArgTypes>

\_\_device\_\_ \_\_host\_\_

bool operator!=(const function<\_R(\_ArgTypes...)>&, nullptr\_t) noexcept;

template <class \_R, class... \_ArgTypes>

\_\_device\_\_ \_\_host\_\_

bool operator!=(nullptr\_t, const function<\_R(\_ArgTypes...)>&) noexcept;

// specialized algorithms

template <class \_R, class... \_ArgTypes>

\_\_device\_\_ \_\_host\_\_

void swap(function<\_R(\_ArgTypes...)>&, function<\_R(\_ArgTypes...)>&);

}

## [F. Texture Fetching](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "texture-fetching)

This appendix gives the formula used to compute the value returned by the texture functions of [Texture Functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texture-functions) depending on the various attributes of the texture reference (see [Texture and Surface Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texture-and-surface-memory)).

The texture bound to the texture reference is represented as an array T of

* N texels for a one-dimensional texture,
* N x M texels for a two-dimensional texture,
* N x M x L texels for a three-dimensional texture.

It is fetched using non-normalized texture coordinates x, y, and z, or the normalized texture coordinates x/N, y/M, and z/L as described in [Texture Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texture-memory). In this appendix, the coordinates are assumed to be in the valid range. [Texture Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texture-memory) explained how out-of-range coordinates are remapped to the valid range based on the addressing mode.

### [F.1. Nearest-Point Sampling](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "nearest-point-sampling)

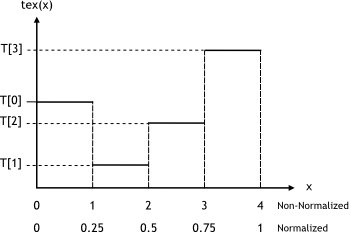
In this filtering mode, the value returned by the texture fetch is

* tex(x)=T[i] for a one-dimensional texture,
* tex(x,y)=T[i,j] for a two-dimensional texture,
* tex(x,y,z)=T[i,j,k] for a three-dimensional texture,

where i=floor(x), j=floor(y), and k=floor(z).

[Figure 13](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#nearest-point-sampling__nearest-point-sampling-fig) illustrates nearest-point sampling for a one-dimensional texture with N=4.

For integer textures, the value returned by the texture fetch can be optionally remapped to [0.0, 1.0] (see [Texture Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texture-memory)).

Figure 13. Nearest-Point Sampling Filtering Mode. Nearest-point sampling of a one-dimensional texture of four texels.  
  


### [F.2. Linear Filtering](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "linear-filtering)

In this filtering mode, which is only available for floating-point textures, the value returned by the texture fetch is

* tex(x)=(1−α)T[i]+αT[i+1] for a one-dimensional texture,
* tex(x,y)=(1−α)(1−β)T[i,j]+α(1−β)T[i+1,j]+(1−α)βT[i,j+1]+αβT[i+1,j+1] for a two-dimensional texture,
* tex(x,y,z) =

(1−α)(1−β)(1−γ)T[i,j,k]+α(1−β)(1−γ)T[i+1,j,k]+

(1−α)β(1−γ)T[i,j+1,k]+αβ(1−γ)T[i+1,j+1,k]+

(1−α)(1−β)γT[i,j,k+1]+α(1−β)γT[i+1,j,k+1]+

(1−α)βγT[i,j+1,k+1]+αβγT[i+1,j+1,k+1]

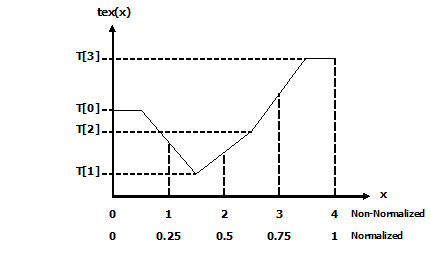
for a three-dimensional texture,

where:

* i=floor(xB), α=frac(xB), xB=x-0.5,
* j=floor(yB), β=frac(yB), yB=y-0.5,
* k=floor(zB), γ=frac(zB), zB= z-0.5,

α, β, and γ are stored in 9-bit fixed point format with 8 bits of fractional value (so 1.0 is exactly represented).

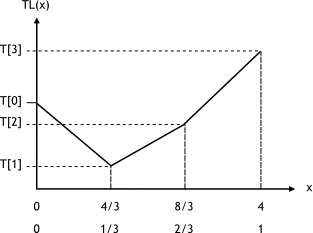
[Figure 14](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#linear-filtering__linear-filtering-of-1-d-texture-of-4-texels) illustrates linear filtering of a one-dimensional texture with N=4.

Figure 14. Linear Filtering Mode. Linear filtering of a one-dimensional texture of four texels in clamp addressing mode.  
  


### [F.3. Table Lookup](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "table-lookup)

A table lookup TL(x) where x spans the interval [0,R] can be implemented as TL(x)=tex((N-1)/R)x+0.5) in order to ensure that TL(0)=T[0] and TL(R)=T[N-1].

[Figure 15](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#table-lookup__1-d-table-lookup-using-linear-filtering) illustrates the use of texture filtering to implement a table lookup with R=4 or R=1 from a one-dimensional texture with N=4.

Figure 15. One-Dimensional Table Lookup Using Linear Filtering  
  


## [G. Compute Capabilities](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "compute-capabilities)

The general specifications and features of a compute device depend on its compute capability (see [Compute Capability](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compute-capability)).

[Table 11](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#features-and-technical-specifications__feature-support-per-compute-capability) gives the features and technical specifications associated to each compute capability.

[Floating-Point Standard](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#floating-point-standard) reviews the compliance with the IEEE floating-point standard.

Sections [Compute Capability 2.x](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compute-capability-2-x), [Compute Capability 3.x](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compute-capability-3-0), and [Compute Capability 5.x](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compute-capability-5-x) give more details on the architecture of devices of compute capability 2.x, 3.x, and 5.x, respectively.

### [G.1. Features and Technical Specifications](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "features-and-technical-specifications)

| Table 11. Feature Support per Compute Capability | | | | | | | | | | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Feature Support** | | | **Compute Capability** | | | | | | | |
| **(Unlisted features are supported for all compute capabilities)** | | | **2.x** | | **3.0** | | **3.2** | | **3.5, 3.7, 5.x** | |
| Atomic functions operating on 32-bit integer values in global memory ([Atomic Functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#atomic-functions)) | | | Yes | | | | | | | |
| atomicExch() operating on 32-bit floating point values in global memory ([atomicExch()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#atomicexch)) | | |
| Atomic functions operating on 32-bit integer values in shared memory ([Atomic Functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#atomic-functions)) | | |
| atomicExch() operating on 32-bit floating point values in shared memory ([atomicExch()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#atomicexch)) | | |
| Atomic functions operating on 64-bit integer values in global memory ([Atomic Functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#atomic-functions)) | | |
| Warp vote functions ([Warp Vote Functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#warp-vote-functions)) | | |
| Double-precision floating-point numbers | | |
| Atomic functions operating on 64-bit integer values in shared memory ([Atomic Functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#atomic-functions)) | | |
| Atomic addition operating on 32-bit floating point values in global and shared memory ([atomicAdd()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#atomicadd)) | | |
| \_\_ballot() ([Warp Vote Functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#warp-vote-functions)) | | |
| \_\_threadfence\_system() ([Memory Fence Functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#memory-fence-functions)) | | |
| \_\_syncthreads\_count(),  \_\_syncthreads\_and(),  \_\_syncthreads\_or() ([Synchronization Functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#synchronization-functions)) | | |
| Surface functions ([Surface Functions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#surface-functions)) | | |
| 3D grid of thread blocks | | |
| Unified Memory Programming | | | No | | Yes | | | | | |
| Funnel shift (see reference manual) | | | No | | | | Yes | | | |
| Dynamic Parallelism | | | No | | | | | | Yes | |
| Table 12. Technical Specifications per Compute Capability | | | | | | | | | | |
|  | **Compute Capability** | | | | | | | | | |
| **Technical Specifications** | **2.x** | **3.0** | | **3.2, 3.5** | | **3.7** | | **5.0** | | **5.2** |
| Maximum dimensionality of grid of thread blocks | 3 | | | | | | | | | |
| Maximum x-dimension of a grid of thread blocks | 65535 | 231-1 | | | | | | | | |
| Maximum y- or z-dimension of a grid of thread blocks | 65535 | | | | | | | | | |
| Maximum dimensionality of thread block | 3 | | | | | | | | | |
| Maximum x- or y-dimension of a block | 1024 | | | | | | | | | |
| Maximum z-dimension of a block | 64 | | | | | | | | | |
| Maximum number of threads per block | 1024 | | | | | | | | | |
| Warp size | 32 | | | | | | | | | |
| Maximum number of resident blocks per multiprocessor | 8 | 16 | | | | | | 32 | | |
| Maximum number of resident warps per multiprocessor | 48 | 64 | | | | | | | | |
| Maximum number of resident threads per multiprocessor | 1536 | 2048 | | | | | | | | |
| Number of 32-bit registers per multiprocessor | 32 K | 64 K | | | | 128 K | | 64 K | | |
| Maximum number of 32-bit registers per thread block | 32 K | 64 K | | | | | | | | |
| Maximum number of 32-bit registers per thread | 63 | | | 255 | | | | | | |
| Maximum amount of shared memory per multiprocessor | 48 KB | | | | | 112 KB | | 64 KB | | 96 KB |
| Maximum amount of shared memory per thread block | 48 KB | | | | | | | | | |
| Number of shared memory banks | 32 | | | | | | | | | |
| Amount of local memory per thread | 512 KB | | | | | | | | | |
| Constant memory size | 64 KB | | | | | | | | | |
| Cache working set per multiprocessor for constant memory | 8 KB | | | | | | | 10 KB | | |
| Cache working set per multiprocessor for texture memory | 12 KB | Between 12 KB and 48 KB | | | | | | | | |
| Maximum width for a 1D texture reference bound to a CUDA array | 65536 | | | | | | | | | |
| Maximum width for a 1D texture reference bound to linear memory | 227 | | | | | | | | | |
| Maximum width and number of layers for a 1D layered texture reference | 16384 x 2048 | | | | | | | | | |
| Maximum width and height for a 2D texture reference bound to a CUDA array | 65536 x 65535 | | | | | | | | | |
| Maximum width and height for a 2D texture reference bound to linear memory | 65000 x 65000 | | | | | | | | | |
| Maximum width and height for a 2D texture reference bound to a CUDA array supporting texture gather | 16384 x 16384 | | | | | | | | | |
| Maximum width, height, and number of layers for a 2D layered texture reference | 16384 x 16384 x 2048 | | | | | | | | | |
| Maximum width, height, and depth for a 3D texture reference bound to a CUDA array | 2048 x 2048 x 2048 | 4096 x 4096 x 4096 | | | | | | | | |
| Maximum width (and height) for a cubemap texture reference | 16384 | | | | | | | | | |
| Maximum width (and height) and number of layers for a cubemap layered texture reference | 16384 x 2046 | | | | | | | | | |
| Maximum number of textures that can be bound to a kernel | 128 | 256 | | | | | | | | |
| Maximum width for a 1D surface reference bound to a CUDA array | 65536 | | | | | | | | | |
| Maximum width and number of layers for a 1D layered surface reference | 65536 x 2048 | | | | | | | | | |
| Maximum width and height for a 2D surface reference bound to a CUDA array | 65536 x 32768 | | | | | | | | | |
| Maximum width, height, and number of layers for a 2D layered surface reference | 65536 x 32768 x 2048 | | | | | | | | | |
| Maximum width, height, and depth for a 3D surface reference bound to a CUDA array | 65536 x 32768 x 2048 | | | | | | | | | |
| Maximum width (and height) for a cubemap surface reference bound to a CUDA array | 32768 | | | | | | | | | |
| Maximum width (and height) and number of layers for a cubemap layered surface reference | 32768 x 2046 | | | | | | | | | |
| Maximum number of surfaces that can be bound to a kernel | 8 | 16 | | | | | | | | |
| Maximum number of instructions per kernel | 512 million | | | | | | | | | |

### [G.2. Floating-Point Standard](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "floating-point-standard)

All compute devices follow the IEEE 754-2008 standard for binary floating-point arithmetic with the following deviations:

* There is no dynamically configurable rounding mode; however, most of the operations support multiple IEEE rounding modes, exposed via device intrinsics;
* There is no mechanism for detecting that a floating-point exception has occurred and all operations behave as if the IEEE-754 exceptions are always masked, and deliver the masked response as defined by IEEE-754 if there is an exceptional event; for the same reason, while SNaN encodings are supported, they are not signaling and are handled as quiet;
* The result of a single-precision floating-point operation involving one or more input NaNs is the quiet NaN of bit pattern 0x7fffffff;
* Double-precision floating-point absolute value and negation are not compliant with IEEE-754 with respect to NaNs; these are passed through unchanged;

Code must be compiled with -ftz=false, -prec-div=true, and -prec-sqrt=true to ensure IEEE compliance (this is the default setting; see the nvcc user manual for description of these compilation flags).

Regardless of the setting of the compiler flag -ftz,

* Atomic single-precision floating-point adds on global memory always operate in flush-to-zero mode, i.e., behave equivalent to FADD.F32.FTZ.RN,
* Atomic single-precision floating-point adds on shared memory always operate with denormal support, i.e., behave equivalent to FADD.F32.RN.

In accordance to the IEEE-754R standard, if one of the input parameters to fminf(), fmin(), fmaxf(), or fmax() is NaN, but not the other, the result is the non-NaN parameter.

The conversion of a floating-point value to an integer value in the case where the floating-point value falls outside the range of the integer format is left undefined by IEEE-754. For compute devices, the behavior is to clamp to the end of the supported range. This is unlike the x86 architecture behavior.

The behavior of integer division by zero and integer overflow is left undefined by IEEE-754. For compute devices, there is no mechanism for detecting that such integer operation exceptions have occurred. Integer division by zero yields an unspecified, machine-specific value.

<http://developer.nvidia.com/content/precision-performance-floating-point-and-ieee-754-compliance-nvidia-gpus> includes more information on the floating point accuracy and compliance of NVIDIA GPUs.

### [G.3. Compute Capability 2.x](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "compute-capability-2-x)

### [G.3.1. Architecture](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "architecture-2-x)

For devices of compute capability 2.x, a multiprocessor consists of:

* For devices of compute capability 2.0:
  + 32 CUDA cores for arithmetic operations (see [Arithmetic Instructions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#arithmetic-instructions) for throughputs of arithmetic operations),
  + 4 special function units for single-precision floating-point transcendental functions,
* For devices of compute capability 2.1:
  + 48 CUDA cores for arithmetic operations (see [Arithmetic Instructions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#arithmetic-instructions) for throughputs of arithmetic operations),
  + 8 special function units for single-precision floating-point transcendental functions,
* 2 warp schedulers.

At every instruction issue time, each scheduler issues:

* One instruction for devices of compute capability 2.0,
* Two independent instructions for devices of compute capability 2.1,

for some warp that is ready to execute, if any. The first scheduler is in charge of the warps with an odd ID and the second scheduler is in charge of the warps with an even ID. Note that when a scheduler issues a double-precision floating-point instruction, the other scheduler cannot issue any instruction.

A warp scheduler can issue an instruction to only half of the CUDA cores. To execute an instruction for all threads of a warp, a warp scheduler must therefore issue the instruction over two clock cycles for an integer or floating-point arithmetic instruction.

A multiprocessor also has a read-only constant cache that is shared by all functional units and speeds up reads from the constant memory space, which resides in device memory.

There is an L1 cache for each multiprocessor and an L2 cache shared by all multiprocessors, both of which are used to cache accesses to local or global memory, including temporary register spills. The cache behavior (e.g., whether reads are cached in both L1 and L2 or in L2 only) can be partially configured on a per-access basis using modifiers to the load or store instruction.

The same on-chip memory is used for both L1 and shared memory: It can be configured as 48 KB of shared memory and 16 KB of L1 cache or as 16 KB of shared memory and 48 KB of L1 cache, using cudaFuncSetCacheConfig()/cuFuncSetCacheConfig():

// Device code

\_\_global\_\_ void MyKernel(int\* foo, int\* bar, int a)

{

...

}

// Host code

// Runtime API

// cudaFuncCachePreferShared: shared memory is 48 KB

// cudaFuncCachePreferL1: shared memory is 16 KB

// cudaFuncCachePreferNone: no preference

cudaFuncSetCacheConfig(MyKernel, cudaFuncCachePreferShared)

// Or via a function pointer:

void (\*funcPtr)(int\*, int\*, int);

funcPtr = MyKernel;

cudaFuncSetCacheConfig(\*funcPtr, cudaFuncCachePreferShared);

The default cache configuration is "prefer none," meaning "no preference." If a kernel is configured to have no preference, then it will default to the preference of the current thread/context, which is set using cudaDeviceSetCacheConfig()/cuCtxSetCacheConfig() (see the reference manual for details). If the current thread/context also has no preference (which is again the default setting), then whichever cache configuration was most recently used for any kernel will be the one that is used, unless a different cache configuration is required to launch the kernel (e.g., due to shared memory requirements). The initial configuration is 48 KB of shared memory and 16 KB of L1 cache.

Applications may query the L2 cache size by checking the l2CacheSize device property (see [Device Enumeration](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#device-enumeration)). The maximum L2 cache size is 768 KB.

Multiprocessors are grouped into Graphics Processor Clusters (GPCs). A GPC includes four multiprocessors.

Each multiprocessor has a read-only texture cache to speed up reads from the texture memory space, which resides in device memory. It accesses the texture cache via a texture unit that implements the various addressing modes and data filtering mentioned in [Texture and Surface Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texture-and-surface-memory).

### [G.3.2. Global Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "global-memory-2-x)

Global memory accesses are cached. Using the -dlcm compilation flag, they can be configured at compile time to be cached in both L1 and L2 (-Xptxas -dlcm=ca) (this is the default setting) or in L2 only (-Xptxas -dlcm=cg).

A cache line is 128 bytes and maps to a 128 byte aligned segment in device memory. Memory accesses that are cached in both L1 and L2 are serviced with 128-byte memory transactions whereas memory accesses that are cached in L2 only are serviced with 32-byte memory transactions. Caching in L2 only can therefore reduce over-fetch, for example, in the case of scattered memory accesses.

If the size of the words accessed by each thread is more than 4 bytes, a memory request by a warp is first split into separate 128-byte memory requests that are issued independently:

* Two memory requests, one for each half-warp, if the size is 8 bytes,
* Four memory requests, one for each quarter-warp, if the size is 16 bytes.

Each memory request is then broken down into cache line requests that are issued independently. A cache line request is serviced at the throughput of L1 or L2 cache in case of a cache hit, or at the throughput of device memory, otherwise.

Note that threads can access any words in any order, including the same words.

If a non-atomic instruction executed by a warp writes to the same location in global memory for more than one of the threads of the warp, only one thread performs a write and which thread does it is undefined.

[Figure 16](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#global-memory-3-0__examples-of-global-memory-accesses) shows some examples of global memory accesses and corresponding memory transactions.

### [G.3.3. Shared Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "shared-memory-2-x)

Shared memory has 32 banks that are organized such that successive 32-bit words map to successive banks. Each bank has a bandwidth of 32 bits per two clock cycles.

A shared memory request for a warp does not generate a bank conflict between two threads that access any address within the same 32-bit word (even though the two addresses fall in the same bank): In that case, for read accesses, the word is broadcast to the requesting threads (multiple words can be broadcast in a single transaction) and for write accesses, each address is written by only one of the threads (which thread performs the write is undefined).

This means, in particular, that there are no bank conflicts if an array of char is accessed as follows, for example:

extern \_\_shared\_\_ char shared[];

char data = shared[BaseIndex + tid];

[Figure 18](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#shared-memory-5-x__examples-of-irregular-shared-memory-accesses) shows some examples of memory read accesses that involve the broadcast mechanism for devices of compute capability 3.x. The same examples apply for devices of compute capability 2.x.

#### 32-Bit Strided Access

A common access pattern is for each thread to access a 32-bit word from an array indexed by the thread ID tid and with some stride s:

extern \_\_shared\_\_ float shared[];

float data = shared[BaseIndex + s \* tid];

In this case, threads tid and tid+n access the same bank whenever s\*n is a multiple of the number of banks (i.e., 32) or, equivalently, whenever n is a multiple of 32/d where d is the greatest common divisor of 32 and s. As a consequence, there will be no bank conflict only if the warp size (i.e., 32) is less than or equal to 32/d, i.e., only if d is equal to 1, i.e., s is odd.

[Figure 17](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#shared-memory-5-x__examples-of-strided-shared-memory-accesses) shows some examples of strided access for devices of compute capability 3.x. The same examples apply for devices of compute capability 2.x. However, the access pattern for the example in the middle generates 2-way bank conflicts for devices of compute capability 2.x.

#### Larger Than 32-Bit Access

64-bit and 128-bit accesses are specifically handled to minimize bank conflicts as described below.

Other accesses larger than 32-bit are split into 32-bit, 64-bit, or 128-bit accesses. The following code, for example:

struct type {

float x, y, z;

};

extern \_\_shared\_\_ struct type shared[];

struct type data = shared[BaseIndex + tid];

results in three separate 32-bit reads without bank conflicts since each member is accessed with a stride of three 32-bit words.

**64-Bit Accesses:** For 64-bit accesses, a bank conflict only occurs if two threads in either of the half-warps access different addresses belonging to the same bank.

**128-Bit Accesses:** The majority of 128-bit accesses will cause 2-way bank conflicts, even if no two threads in a quarter-warp access different addresses belonging to the same bank. Therefore, to determine the ways of bank conflicts, one must add 1 to the maximum number of threads in a quarter-warp that access different addresses belonging to the same bank.

### [G.3.4. Constant Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "constant-memory-2-x)

In addition to the constant memory space supported by devices of all compute capabilities (where \_\_constant\_\_ variables reside), devices of compute capability 2.x support the LDU (LoaD Uniform) instruction that the compiler uses to load any variable that is:

* pointing to global memory,
* read-only in the kernel (programmer can enforce this using the const keyword),
* not dependent on thread ID.

### [G.4. Compute Capability 3.x](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "compute-capability-3-0)

### [G.4.1. Architecture](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "architecture-3-0)

A multiprocessor consists of:

* 192 CUDA cores for arithmetic operations (see [Arithmetic Instructions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#arithmetic-instructions) for throughputs of arithmetic operations),
* 32 special function units for single-precision floating-point transcendental functions,
* 4 warp schedulers.

When a multiprocessor is given warps to execute, it first distributes them among the four schedulers. Then, at every instruction issue time, each scheduler issues two independent instructions for one of its assigned warps that is ready to execute, if any.

A multiprocessor has a read-only constant cache that is shared by all functional units and speeds up reads from the constant memory space, which resides in device memory.

There is an L1 cache for each multiprocessor and an L2 cache shared by all multiprocessors. The L1 cache is used to cache accesses to local memory, including temporary register spills. The L2 cache is used to cache accesses to local and global memory. The cache behavior (e.g., whether reads are cached in both L1 and L2 or in L2 only) can be partially configured on a per-access basis using modifiers to the load or store instruction. Some devices of compute capability 3.5 and devices of compute capability 3.7 allow opt-in to caching of global memory in both L1 and L2 via compiler options.

The same on-chip memory is used for both L1 and shared memory: It can be configured as 48 KB of shared memory and 16 KB of L1 cache or as 16 KB of shared memory and 48 KB of L1 cache or as 32 KB of shared memory and 32 KB of L1 cache, using cudaFuncSetCacheConfig()/cuFuncSetCacheConfig():

// Device code

\_\_global\_\_ void MyKernel()

{

...

}

// Host code

// Runtime API

// cudaFuncCachePreferShared: shared memory is 48 KB

// cudaFuncCachePreferEqual: shared memory is 32 KB

// cudaFuncCachePreferL1: shared memory is 16 KB

// cudaFuncCachePreferNone: no preference

cudaFuncSetCacheConfig(MyKernel, cudaFuncCachePreferShared)

The default cache configuration is "prefer none," meaning "no preference." If a kernel is configured to have no preference, then it will default to the preference of the current thread/context, which is set using cudaDeviceSetCacheConfig()/cuCtxSetCacheConfig() (see the reference manual for details). If the current thread/context also has no preference (which is again the default setting), then whichever cache configuration was most recently used for any kernel will be the one that is used, unless a different cache configuration is required to launch the kernel (e.g., due to shared memory requirements). The initial configuration is 48 KB of shared memory and 16 KB of L1 cache.

Note: Devices of compute capability 3.7 add an additional 64 KB of shared memory to each of the above configurations, yielding 112 KB, 96 KB, and 80 KB shared memory per multiprocessor, respectively. However, the maximum shared memory per thread block remains 48 KB.

Applications may query the L2 cache size by checking the l2CacheSize device property (see [Device Enumeration](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#device-enumeration)). The maximum L2 cache size is 1.5 MB.

Multiprocessors are grouped into Graphics Processor Clusters (GPCs). A GPC includes three multiprocessors.

Each multiprocessor has a read-only data cache of 48 KB to speed up reads from device memory. It accesses this cache either directly (for devices of compute capability 3.5 or 3.7), or via a texture unit that implements the various addressing modes and data filtering mentioned in [Texture and Surface Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texture-and-surface-memory). When accessed via the texture unit, the read-only data cache is also referred to as texture cache.

### [G.4.2. Global Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "global-memory-3-0)

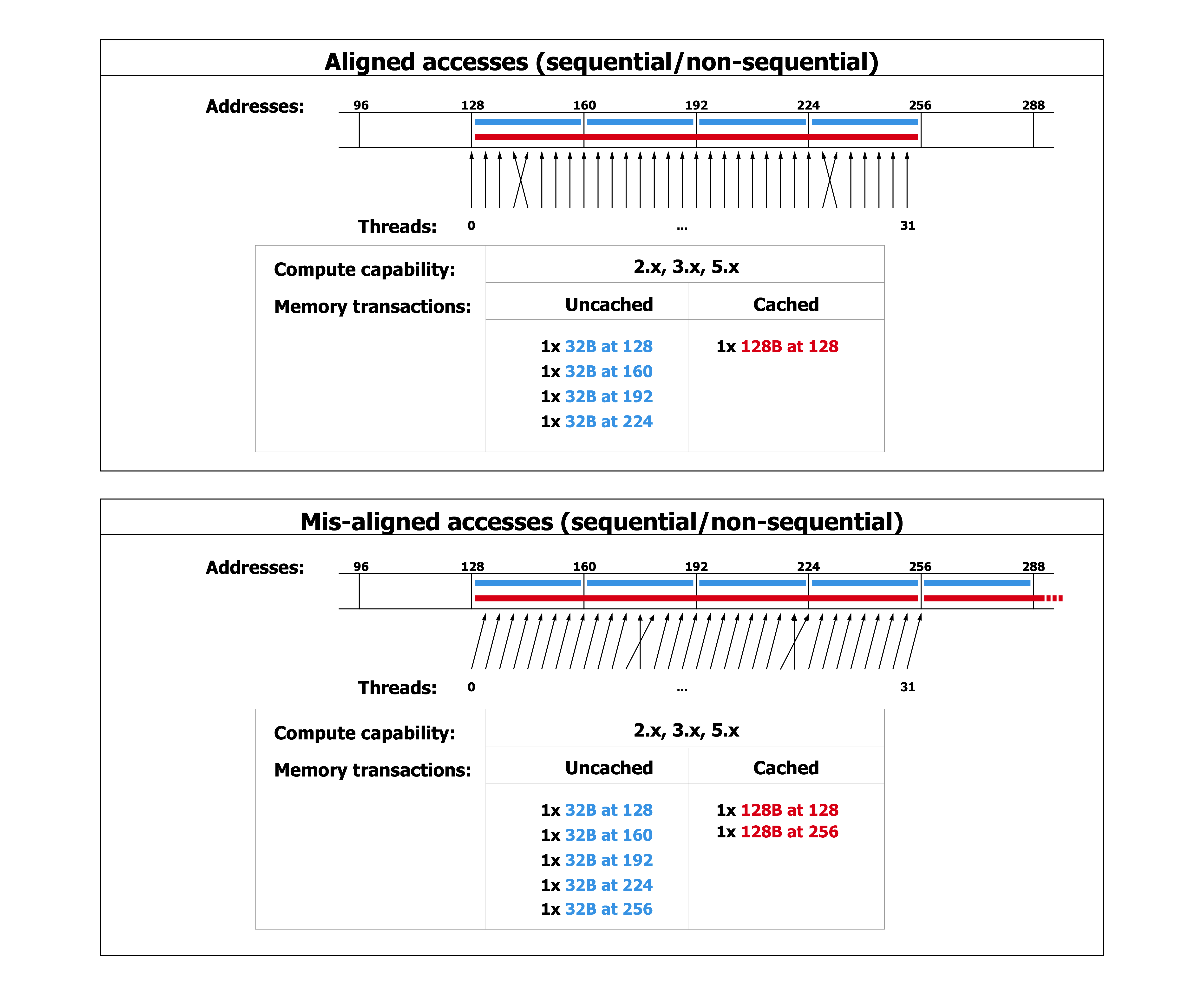
Global memory accesses for devices of compute capability 3.x are cached in L2 and for devices of compute capability 3.5 or 3.7, may also be cached in the read-only data cache described in the previous section; they are normally not cached in L1. Some devices of compute capability 3.5 and devices of compute capability 3.7 allow opt-in to caching of global memory accesses in L1 via the -Xptxas -dlcm=ca option to nvcc.

Caching in L2 behaves in the same way as for devices of compute capability 2.x (see [Global Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#global-memory-2-x)).

Data that is read-only for the entire lifetime of the kernel can also be cached in the read-only data cache described in the previous section by reading it using the \_\_ldg() function (see [Read-Only Data Cache Load Function](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#ldg-function)). When the compiler detects that the read-only condition is satisfied for some data, it will use \_\_ldg() to read it. The compiler might not always be able to detect that the read-only condition is satisfied for some data. Marking pointers used for loading such data with both the const and \_\_restrict\_\_ qualifiers increases the likelihood that the compiler will detect the read-only condition.

[Figure 16](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#global-memory-3-0__examples-of-global-memory-accesses) shows some examples of global memory accesses and corresponding memory transactions.

Figure 16. Examples of Global Memory Accesses. Examples of Global Memory Accesses by a Warp, 4-Byte Word per Thread, and Associated Memory Transactions for Compute Capabilities 2.x and Beyond



### [G.4.3. Shared Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "shared-memory-3-0)

Shared memory has 32 banks with two addressing modes that are described below.

The addressing mode can be queried using cudaDeviceGetSharedMemConfig() and set using cudaDeviceSetSharedMemConfig() (see reference manual for more details). Each bank has a bandwidth of 64 bits per clock cycle.

[Figure 17](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#shared-memory-5-x__examples-of-strided-shared-memory-accesses) shows some examples of strided access.

[Figure 18](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#shared-memory-5-x__examples-of-irregular-shared-memory-accesses) shows some examples of memory read accesses that involve the broadcast mechanism.

#### 64-Bit Mode

Successive 64-bit words map to successive banks.

A shared memory request for a warp does not generate a bank conflict between two threads that access any sub-word within the same 64-bit word (even though the addresses of the two sub-words fall in the same bank): In that case, for read accesses, the 64-bit word is broadcast to the requesting threads and for write accesses, each sub-word is written by only one of the threads (which thread performs the write is undefined).

In this mode, the same access pattern generates fewer bank conflicts than on devices of compute capability 2.x for 64-bit accesses and as many or fewer for 32-bit accesses.

#### 32-Bit Mode

Successive 32-bit words map to successive banks.

A shared memory request for a warp does not generate a bank conflict between two threads that access any sub-word within the same 32-bit word or within two 32-bit words whose indices i and j are in the same 64-word aligned segment (i.e., a segment whose first index is a multiple of 64) and such that j=i+32 (even though the addresses of the two sub-words fall in the same bank): In that case, for read accesses, the 32-bit words are broadcast to the requesting threads and for write accesses, each sub-word is written by only one of the threads (which thread performs the write is undefined).

In this mode, the same access pattern generates as many or fewer bank conflicts than on devices of compute capability 2.x.

### [G.5. Compute Capability 5.x](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "compute-capability-5-x)

### [G.5.1. Architecture](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "architecture-5-x)

A multiprocessor consists of:

* 128 CUDA cores for arithmetic operations (see [Arithmetic Instructions](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#arithmetic-instructions) for throughputs of arithmetic operations),
* 32 special function units for single-precision floating-point transcendental functions,
* 4 warp schedulers.

When a multiprocessor is given warps to execute, it first distributes them among the four schedulers. Then, at every instruction issue time, each scheduler issues one instruction for one of its assigned warps that is ready to execute, if any.

A multiprocessor has:

* a read-only constant cache that is shared by all functional units and speeds up reads from the constant memory space, which resides in device memory,
* a unified L1/texture cache of 24 KB used to cache reads from global memory,
* 64 KB of shared memory for devices of compute capability 5.0 or 96 KB of shared memory for devices of compute capability 5.2.

The unified L1/texture cache is also used by the texture unit that implements the various addressing modes and data filtering mentioned in [Texture and Surface Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#texture-and-surface-memory).

There is also an L2 cache shared by all multiprocessors that is used to cache accesses to local or global memory, including temporary register spills. Applications may query the L2 cache size by checking the l2CacheSize device property (see [Device Enumeration](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#device-enumeration)).

The cache behavior (e.g., whether reads are cached in both the unified L1/texture cache and L2 or in L2 only) can be partially configured on a per-access basis using modifiers to the load instruction.

Multiprocessors are grouped into Graphics Processor Clusters (GPCs). A GPC includes four multiprocessors.

### [G.5.2. Global Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "global-memory-5-x)

Global memory accesses are always cached in L2 and caching in L2 behaves in the same way as for devices of compute capability 2.x (see [Global Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#global-memory-2-x)).

Data that is read-only for the entire lifetime of the kernel can also be cached in the unified L1/texture cache described in the previous section by reading it using the \_\_ldg() function (see [Read-Only Data Cache Load Function](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#ldg-function)). When the compiler detects that the read-only condition is satisfied for some data, it will use \_\_ldg() to read it. The compiler might not always be able to detect that the read-only condition is satisfied for some data. Marking pointers used for loading such data with both the const and \_\_restrict\_\_ qualifiers increases the likelihood that the compiler will detect the read-only condition.

Data that is not read-only for the entire lifetime of the kernel cannot be cached in the unified L1/texture cache for devices of compute capability 5.0. For devices of compute capability 5.2, it is, by default, not cached in the unified L1/texture cache, but caching may be enabled using the following mechanisms:

* Perform the read using inline assembly with the appropriate modifier as described in the PTX reference manual;
* Compile with the -Xptxas -dlcm=ca compilation flag, in which case all reads are cached, except reads that are performed using inline assembly with a modifier that disables caching;
* Compile with the -Xptxas -fscm=ca compilation flag, in which case all reads are cached, including reads that are performed using inline assembly regardless of the modifier used.

When caching is enabled using some the three mechanisms listed above, devices of compute capability 5.2 will cache global memory reads in the unified L1/texture cache for all kernel launches except for the kernel launches for which thread blocks consume too much of the multiprocessor's resources. These exceptions are reported by the profiler.

### [G.5.3. Shared Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "shared-memory-5-x)

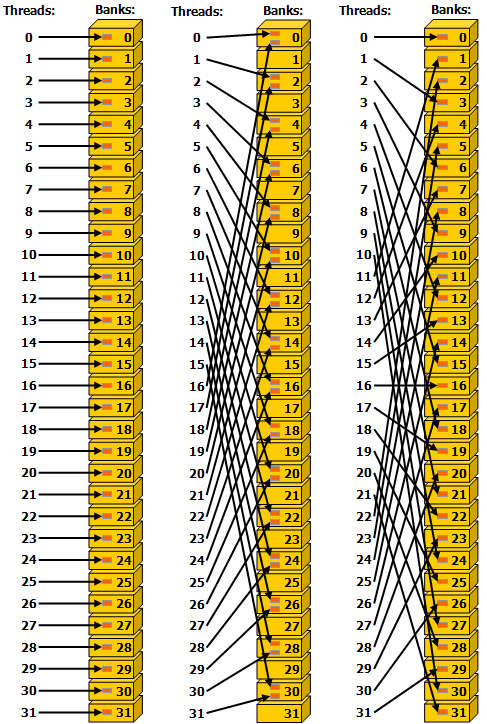
Shared memory has 32 banks that are organized such that successive 32-bit words map to successive banks. Each bank has a bandwidth of 32 bits per clock cycle.

A shared memory request for a warp does not generate a bank conflict between two threads that access any address within the same 32-bit word (even though the two addresses fall in the same bank): In that case, for read accesses, the word is broadcast to the requesting threads and for write accesses, each address is written by only one of the threads (which thread performs the write is undefined).

[Figure 17](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#shared-memory-5-x__examples-of-strided-shared-memory-accesses) shows some examples of strided access.

[Figure 18](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#shared-memory-5-x__examples-of-irregular-shared-memory-accesses) shows some examples of memory read accesses that involve the broadcast mechanism.

Figure 17. Strided Shared Memory Accesses. Examples for devices of compute capability 3.x (in 32-bit mode) or compute capability 5.x.



Left

Linear addressing with a stride of one 32-bit word (no bank conflict).

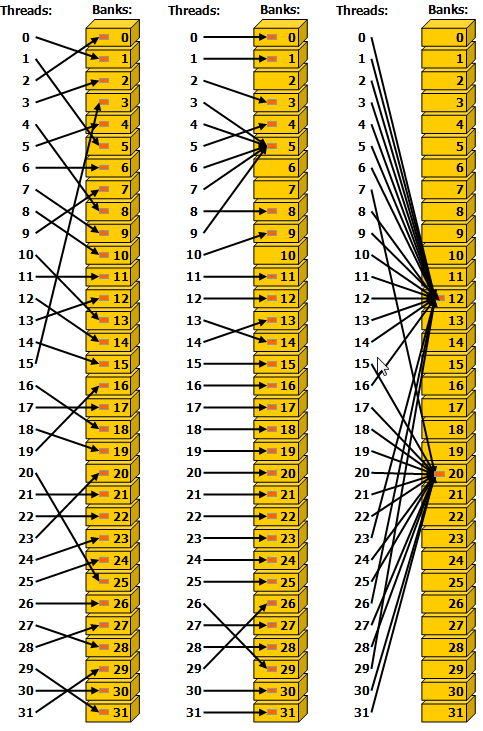
Middle

Linear addressing with a stride of two 32-bit words (two-way bank conflict).

Right

Linear addressing with a stride of three 32-bit words (no bank conflict).

Figure 18. Irregular Shared Memory Accesses. Examples for devices of compute capability 3.x or 5.x.



Left

Conflict-free access via random permutation.

Middle

Conflict-free access since threads 3, 4, 6, 7, and 9 access the same word within bank 5.

Right

Conflict-free broadcast access (threads access the same word within a bank).

## [H. Driver API](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "driver-api)

This appendix assumes knowledge of the concepts described in [CUDA C Runtime](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#cuda-c-runtime).

The driver API is implemented in the cuda dynamic library (cuda.dll or cuda.so) which is copied on the system during the installation of the device driver. All its entry points are prefixed with cu.

It is a handle-based, imperative API: Most objects are referenced by opaque handles that may be specified to functions to manipulate the objects.

The objects available in the driver API are summarized in [Table 13](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#driver-api__objects-available-in-cuda-driver-api).

| Table 13. Objects Available in the CUDA Driver API | | |
| --- | --- | --- |
| **Object** | **Handle** | **Description** |
| Device | CUdevice | CUDA-enabled device |
| Context | CUcontext | Roughly equivalent to a CPU process |
| Module | CUmodule | Roughly equivalent to a dynamic library |
| Function | CUfunction | Kernel |
| Heap memory | CUdeviceptr | Pointer to device memory |
| CUDA array | CUarray | Opaque container for one-dimensional or two-dimensional data on the device, readable via texture or surface references |
| Texture reference | CUtexref | Object that describes how to interpret texture memory data |
| Surface reference | CUsurfref | Object that describes how to read or write CUDA arrays |
| Event | CUevent | Object that describes a CUDA event |

The driver API must be initialized with cuInit() before any function from the driver API is called. A CUDA context must then be created that is attached to a specific device and made current to the calling host thread as detailed in [Context](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#context).

Within a CUDA context, kernels are explicitly loaded as PTX or binary objects by the host code as described in [Module](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#module). Kernels written in C must therefore be compiled separately into PTX or binary objects. Kernels are launched using API entry points as described in [Kernel Execution](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#kernel-execution).

Any application that wants to run on future device architectures must load PTX, not binary code. This is because binary code is architecture-specific and therefore incompatible with future architectures, whereas PTX code is compiled to binary code at load time by the device driver.

Here is the host code of the sample from [Kernels](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#kernels) written using the driver API:

int main()

{

int N = ...;

size\_t size = N \* sizeof(float);

// Allocate input vectors h\_A and h\_B in host memory

float\* h\_A = (float\*)malloc(size);

float\* h\_B = (float\*)malloc(size);

// Initialize input vectors

...

// Initialize

cuInit(0);

// Get number of devices supporting CUDA

int deviceCount = 0;

cuDeviceGetCount(&deviceCount);

if (deviceCount == 0) {

printf("There is no device supporting CUDA.\n");

exit (0);

}

// Get handle for device 0

CUdevice cuDevice;

cuDeviceGet(&cuDevice, 0);

// Create context

CUcontext cuContext;

cuCtxCreate(&cuContext, 0, cuDevice);

// Create module from binary file

CUmodule cuModule;

cuModuleLoad(&cuModule, "VecAdd.ptx");

// Allocate vectors in device memory

CUdeviceptr d\_A;

cuMemAlloc(&d\_A, size);

CUdeviceptr d\_B;

cuMemAlloc(&d\_B, size);

CUdeviceptr d\_C;

cuMemAlloc(&d\_C, size);

// Copy vectors from host memory to device memory

cuMemcpyHtoD(d\_A, h\_A, size);

cuMemcpyHtoD(d\_B, h\_B, size);

// Get function handle from module

CUfunction vecAdd;

cuModuleGetFunction(&vecAdd, cuModule, "VecAdd");

// Invoke kernel

int threadsPerBlock = 256;

int blocksPerGrid =

(N + threadsPerBlock - 1) / threadsPerBlock;

void\* args[] = { &d\_A, &d\_B, &d\_C, &N };

cuLaunchKernel(vecAdd,

blocksPerGrid, 1, 1, threadsPerBlock, 1, 1,

0, 0, args, 0);

...

}

Full code can be found in the vectorAddDrv CUDA sample.

### [H.1. Context](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "context)

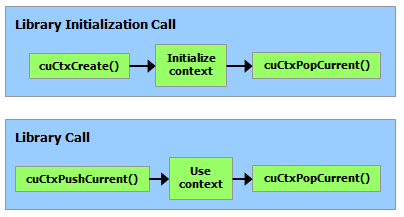
A CUDA context is analogous to a CPU process. All resources and actions performed within the driver API are encapsulated inside a CUDA context, and the system automatically cleans up these resources when the context is destroyed. Besides objects such as modules and texture or surface references, each context has its own distinct address space. As a result, CUdeviceptr values from different contexts reference different memory locations.

A host thread may have only one device context current at a time. When a context is created with cuCtxCreate(), it is made current to the calling host thread. CUDA functions that operate in a context (most functions that do not involve device enumeration or context management) will return CUDA\_ERROR\_INVALID\_CONTEXT if a valid context is not current to the thread.

Each host thread has a stack of current contexts. cuCtxCreate() pushes the new context onto the top of the stack. cuCtxPopCurrent() may be called to detach the context from the host thread. The context is then "floating" and may be pushed as the current context for any host thread. cuCtxPopCurrent() also restores the previous current context, if any.

A usage count is also maintained for each context. cuCtxCreate() creates a context with a usage count of 1. cuCtxAttach() increments the usage count and cuCtxDetach() decrements it. A context is destroyed when the usage count goes to 0 when calling cuCtxDetach() or cuCtxDestroy().

Usage count facilitates interoperability between third party authored code operating in the same context. For example, if three libraries are loaded to use the same context, each library would call cuCtxAttach() to increment the usage count and cuCtxDetach() to decrement the usage count when the library is done using the context. For most libraries, it is expected that the application will have created a context before loading or initializing the library; that way, the application can create the context using its own heuristics, and the library simply operates on the context handed to it. Libraries that wish to create their own contexts - unbeknownst to their API clients who may or may not have created contexts of their own - would use cuCtxPushCurrent() and cuCtxPopCurrent() as illustrated in [Figure 19](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#context__library-context-management).

Figure 19. Library Context Management  
  


### [H.2. Module](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "module)

Modules are dynamically loadable packages of device code and data, akin to DLLs in Windows, that are output by nvcc (see [Compilation with NVCC](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compilation-with-nvcc)). The names for all symbols, including functions, global variables, and texture or surface references, are maintained at module scope so that modules written by independent third parties may interoperate in the same CUDA context.

This code sample loads a module and retrieves a handle to some kernel:

CUmodule cuModule;

cuModuleLoad(&cuModule, "myModule.ptx");

CUfunction myKernel;

cuModuleGetFunction(&myKernel, cuModule, "MyKernel");

This code sample compiles and loads a new module from PTX code and parses compilation errors:

#define BUFFER\_SIZE 8192

CUmodule cuModule;

CUjit\_option options[3];

void\* values[3];

char\* PTXCode = "some PTX code";

char error\_log[BUFFER\_SIZE];

int err;

options[0] = CU\_JIT\_ERROR\_LOG\_BUFFER;

values[0] = (void\*)error\_log;

options[1] = CU\_JIT\_ERROR\_LOG\_BUFFER\_SIZE\_BYTES;

values[1] = (void\*)BUFFER\_SIZE;

options[2] = CU\_JIT\_TARGET\_FROM\_CUCONTEXT;

values[2] = 0;

err = cuModuleLoadDataEx(&cuModule, PTXCode, 3, options, values);

if (err != CUDA\_SUCCESS)

printf("Link error:\n%s\n", error\_log);

This code sample compiles, links, and loads a new module from multiple PTX codes and parses link and compilation errors:

#define BUFFER\_SIZE 8192

CUmodule cuModule;

CUjit\_option options[6];

void\* values[6];

float walltime;

char error\_log[BUFFER\_SIZE], info\_log[BUFFER\_SIZE];

char\* PTXCode0 = "some PTX code";

char\* PTXCode1 = "some other PTX code";

CUlinkState linkState;

int err;

void\* cubin;

size\_t cubinSize;

options[0] = CU\_JIT\_WALL\_TIME;

values[0] = (void\*)&walltime;

options[1] = CU\_JIT\_INFO\_LOG\_BUFFER;

values[1] = (void\*)info\_log;

options[2] = CU\_JIT\_INFO\_LOG\_BUFFER\_SIZE\_BYTES;

values[2] = (void\*)BUFFER\_SIZE;

options[3] = CU\_JIT\_ERROR\_LOG\_BUFFER;

values[3] = (void\*)error\_log;

options[4] = CU\_JIT\_ERROR\_LOG\_BUFFER\_SIZE\_BYTES;

values[4] = (void\*)BUFFER\_SIZE;

options[5] = CU\_JIT\_LOG\_VERBOSE;

values[5] = (void\*)1;

cuLinkCreate(6, options, values, &linkState);

err = cuLinkAddData(linkState, CU\_JIT\_INPUT\_PTX,

(void\*)PTXCode0, strlen(PTXCode0) + 1, 0, 0, 0, 0);

if (err != CUDA\_SUCCESS)

printf("Link error:\n%s\n", error\_log);

err = cuLinkAddData(linkState, CU\_JIT\_INPUT\_PTX,

(void\*)PTXCode1, strlen(PTXCode1) + 1, 0, 0, 0, 0);

if (err != CUDA\_SUCCESS)

printf("Link error:\n%s\n", error\_log);

cuLinkComplete(linkState, &cubin, &cubinSize);

printf("Link completed in %fms. Linker Output:\n%s\n", walltime, info\_log);

cuModuleLoadData(cuModule, cubin);

cuLinkDestroy(linkState);

Full code can be found in the ptxjit CUDA sample.

### [H.3. Kernel Execution](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "kernel-execution)

cuLaunchKernel() launches a kernel with a given execution configuration.

Parameters are passed either as an array of pointers (next to last parameter of cuLaunchKernel()) where the nth pointer corresponds to the nth parameter and points to a region of memory from which the parameter is copied, or as one of the extra options (last parameter of cuLaunchKernel()).

When parameters are passed as an extra option (the CU\_LAUNCH\_PARAM\_BUFFER\_POINTER option), they are passed as a pointer to a single buffer where parameters are assumed to be properly offset with respect to each other by matching the alignment requirement for each parameter type in device code.

Alignment requirements in device code for the built-in vector types are listed in [Table 3](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#vector-types__alignment-requirements-in-device-code). For all other basic types, the alignment requirement in device code matches the alignment requirement in host code and can therefore be obtained using \_\_alignof(). The only exception is when the host compiler aligns double and long long (and long on a 64-bit system) on a one-word boundary instead of a two-word boundary (for example, using gcc's compilation flag -mno-align-double) since in device code these types are always aligned on a two-word boundary.

CUdeviceptr is an integer, but represents a pointer, so its alignment requirement is \_\_alignof(void\*).

The following code sample uses a macro (ALIGN\_UP()) to adjust the offset of each parameter to meet its alignment requirement and another macro (ADD\_TO\_PARAM\_BUFFER()) to add each parameter to the parameter buffer passed to the CU\_LAUNCH\_PARAM\_BUFFER\_POINTER option.

#define ALIGN\_UP(offset, alignment) \

(offset) = ((offset) + (alignment) - 1) & ~((alignment) - 1)

char paramBuffer[1024];

size\_t paramBufferSize = 0;

#define ADD\_TO\_PARAM\_BUFFER(value, alignment) \

do { \

paramBufferSize = ALIGN\_UP(paramBufferSize, alignment); \

memcpy(paramBuffer + paramBufferSize, \

&(value), sizeof(value)); \

paramBufferSize += sizeof(value); \

} while (0)

int i;

ADD\_TO\_PARAM\_BUFFER(i, \_\_alignof(i));

float4 f4;

ADD\_TO\_PARAM\_BUFFER(f4, 16); // float4's alignment is 16

char c;

ADD\_TO\_PARAM\_BUFFER(c, \_\_alignof(c));

float f;

ADD\_TO\_PARAM\_BUFFER(f, \_\_alignof(f));

CUdeviceptr devPtr;

ADD\_TO\_PARAM\_BUFFER(devPtr, \_\_alignof(devPtr));

float2 f2;

ADD\_TO\_PARAM\_BUFFER(f2, 8); // float2's alignment is 8

void\* extra[] = {

CU\_LAUNCH\_PARAM\_BUFFER\_POINTER, paramBuffer,

CU\_LAUNCH\_PARAM\_BUFFER\_SIZE, &paramBufferSize,

CU\_LAUNCH\_PARAM\_END

};

cuLaunchKernel(cuFunction,

blockWidth, blockHeight, blockDepth,

gridWidth, gridHeight, gridDepth,

0, 0, 0, extra);

The alignment requirement of a structure is equal to the maximum of the alignment requirements of its fields. The alignment requirement of a structure that contains built-in vector types, CUdeviceptr, or non-aligned double and long long, might therefore differ between device code and host code. Such a structure might also be padded differently. The following structure, for example, is not padded at all in host code, but it is padded in device code with 12 bytes after field f since the alignment requirement for field f4 is 16.

typedef struct {

float f;

float4 f4;

} myStruct;

### [H.4. Interoperability between Runtime and Driver APIs](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "interoperability-between-runtime-and-driver-apis)

An application can mix runtime API code with driver API code.

If a context is created and made current via the driver API, subsequent runtime calls will pick up this context instead of creating a new one.

If the runtime is initialized (implicitly as mentioned in [CUDA C Runtime](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#cuda-c-runtime)), cuCtxGetCurrent() can be used to retrieve the context created during initialization. This context can be used by subsequent driver API calls.

Device memory can be allocated and freed using either API. CUdeviceptr can be cast to regular pointers and vice-versa:

CUdeviceptr devPtr;

float\* d\_data;

// Allocation using driver API

cuMemAlloc(&devPtr, size);

d\_data = (float\*)devPtr;

// Allocation using runtime API

cudaMalloc(&d\_data, size);

devPtr = (CUdeviceptr)d\_data;

In particular, this means that applications written using the driver API can invoke libraries written using the runtime API (such as cuFFT, cuBLAS, ...).

All functions from the device and version management sections of the reference manual can be used interchangeably.

## [I. CUDA Environment Variables](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "env-vars)

Environment variables related to the Multi-Process Service are documented in the Multi-Process Service section of the GPU Deployment and Management guide.

| Table 14. CUDA Environment Variables | | | |
| --- | --- | --- | --- |
| **Category** | **Variable** | **Values** | **Description** |
| Device Enumeration and Properties | CUDA\_​VISIBLE\_​DEVICES | A comma-separated sequence of GPU identifiers | GPU identifiers are given as integer indices or as UUID strings. GPU UUID strings should follow the same format as given by nvidia-smi, such as GPU-8932f937-d72c-4106-c12f-20bd9faed9f6. However, for convenience, abbreviated forms are allowed; simply specify enough digits from the beginning of the GPU UUID to uniquely identify that GPU in the target system. For example, CUDA\_VISIBLE\_DEVICES=GPU-8932f937 may be a valid way to refer to the above GPU UUID, assuming no other GPU in the system shares this prefix.  Only the devices whose index is present in the sequence are visible to CUDA applications and they are enumerated in the order of the sequence. If one of the indices is invalid, only the devices whose index precedes the invalid index are visible to CUDA applications. For example, setting CUDA\_VISIBLE\_DEVICES to 2,1 causes device 0 to be invisible and device 2 to be enumerated before device 1. Setting CUDA\_VISIBLE\_DEVICES to 0,2,-1,1 causes devices 0 and 2 to be visible and device 1 to be invisible. |
| CUDA\_​MANAGED\_​FORCE\_​DEVICE\_​ALLOC | 0 or 1 (default is 0) | Forces the driver to place all managed allocations in device memory. |
| CUDA\_​DEVICE\_​ORDER | FASTEST\_FIRST, PCI\_BUS\_ID, (default is FASTEST\_FIRST) | FASTEST\_FIRST causes CUDA to guess which device is fastest using a simple heuristic, and make that device 0, leaving the order of the rest of the devices unspecified. PCI\_BUS\_ID orders devices by PCI bus ID in ascending order. |
| Compilation | CUDA\_​CACHE\_​DISABLE | 0 or 1 (default is 0) | Disables caching (when set to 1) or enables caching (when set to 0) for just-in-time-compilation. When disabled, no binary code is added to or retrieved from the cache. |
| CUDA\_​CACHE\_​PATH | filepath | Specifies the folder where the just-in-time compiler caches binary codes; the default values are:   * on Windows, %APPDATA%\NVIDIA\ComputeCache, * on MacOS, $HOME/Library/Application\ Support/NVIDIA/ComputeCache, * on Linux, ~/.nv/ComputeCache |
| CUDA\_​CACHE\_​MAXSIZE | integer (default is 33554432 (32 MB) and maximum is 4294967296 (4 GB)) | Specifies the size in bytes of the cache used by the just-in-time compiler. Binary codes whose size exceeds the cache size are not cached. Older binary codes are evicted from the cache to make room for newer binary codes if needed. |
| CUDA\_​FORCE\_​PTX\_​JIT | 0 or 1 (default is 0) | When set to 1, forces the device driver to ignore any binary code embedded in an application (see [Application Compatibility](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#application-compatibility)) and to just-in-time compile embedded PTX code instead. If a kernel does not have embedded PTX code, it will fail to load. This environment variable can be used to validate that PTX code is embedded in an application and that its just-in-time compilation works as expected to guarantee application forward compatibility with future architectures (see [Just-in-Time Compilation](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#just-in-time-compilation)). |
| Execution | CUDA\_​LAUNCH\_​BLOCKING | 0 or 1 (default is 0) | Disables (when set to 1) or enables (when set to 0) asynchronous kernel launches. |
| CUDA\_​DEVICE\_​MAX\_​CONNECTIONS | 1 to 32 (default is 8) | Sets the number of compute and copy engine concurrent connections (work queues) from the host to each device of compute capability 3.5 and above. |
| CUDA\_​AUTO\_​BOOST | 0 or 1 | Overrides the autoboost behavior set by the --auto-boost-default option of nvidia-smi. If an application requests via this environment variable a behavior that is different from nvidia-smi's, its request is honored if there is no other application currently running on the same GPU that successfully requested a different behavior, otherwise it is ignored. |
| cuda-gdb (on Mac and Linux platforms) | CUDA\_​DEVICE\_​WAITS\_​ON\_​EXCEPTION | 0 or 1 (default is 0) | When set to 1, a CUDA application will halt when a device exception occurs, allowing a debugger to be attached for further debugging. |
| Driver-Based Profiler (these variables have no impact on the Visual Profiler or the command line profiler nvprof) | CUDA\_​DEVICE | Integer (default is 0) | Specifies the index of the device to profile. |
| COMPUTE\_​PROFILE | 0 or 1 (default is 0) | Disables profiling (when set to 0) or enables profiling (when set to 1). |
| COMPUTE\_​PROFILE\_​CONFIG | Path | Specifies the configuration file to set profiling options and select performance counters. |
| COMPUTE\_​PROFILE\_​LOG | Path | Specifies the file used to save the profiling output. In case of multiple contexts, use '%d' in the COMPUTE\_PROFILE\_LOG to generate separate output files for each context - with '%d' substituted by the context number. |
| COMPUTE\_​PROFILE\_​CSV | 0 or 1 (default is 0) | When set to 1, the output will be in comma-separated format. |

## [J. Unified Memory Programming](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "um-unified-memory-programming-hd)

### [J.1. Unified Memory Introduction](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "um-introduction)

Unified Memory is a component of the CUDA programming model, first introduced in CUDA 6.0, that defines a new managed memory space in which all processors see a single coherent memory image with a common address space.

Note: A processor refers to any independent execution unit with a dedicated MMU. This includes both CPUs and GPUs of any type and architecture.

The underlying system manages data access and locality within a CUDA program without need for explicit memory copy calls. This benefits GPU programming in two primary ways:

* GPU programming is simplified by unifying memory spaces coherently across all GPUs and CPUs in the system and by providing tighter and more straightforward language integration for CUDA programmers.
* Data access speed is maximized by transparently migrating data towards the processor using it.

In simple terms, Unified Memory eliminates the need for explicit data movement via the cudaMemcpy\*() routines without the performance penalty incurred by placing all data into zero-copy memory. Data movement, of course, still takes place, so a program’s run time typically does not decrease; Unified Memory instead enables the writing of simpler and more maintainable code.

Unified Memory offers a “single-pointer-to-data” model that is conceptually similar to CUDA’s zero-copy memory. One key difference between the two is that with zero-copy allocations the physical location of memory is pinned in CPU system memory such that a program may have fast or slow access to it depending on where it is being accessed from. Unified Memory, on the other hand, decouples memory and execution spaces so that all data accesses are fast.

The term Unified Memory describes as a system that provides memory management services to a wide range of programs, from those targeting the Runtime API down to those using the Virtual ISA (PTX). Part of this system defines the managed memory space that opts in to Unified Memory services.

Managed memory is interoperable and interchangeable with device-specific allocations, such as those created using the cudaMalloc() routine. All CUDA operations that are valid on device memory are also valid on managed memory; the primary difference is that the host portion of a program is able to reference and access the memory as well.

### [J.1.1. Simplifying GPU Programming](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "um-simplifying)

Unification of memory spaces means that there is no longer any need for explicit memory transfers between host and device. Any allocation created in the managed memory space is automatically migrated to where it is needed.

A program allocates managed memory in one of two ways: via the new cudaMallocManaged() routine, which is semantically similar to cudaMalloc(); or by defining a global \_\_managed\_\_ variable, which is semantically similar to a \_\_device\_\_ variable. Precise definitions of these are found later in this document.

The following code examples illustrate how the use of managed memory can change the way in which host code is written. First, a simple program written without the benefit of unified memory:

\_\_global\_\_ void AplusB( int \*ret, int a, int b) {

ret[threadIdx.x] = a + b + threadIdx.x;

}

int main() {

int \*ret;

cudaMalloc(&ret, 1000 \* sizeof(int));

AplusB<<< 1, 1000 >>>(ret, 10, 100);

int \*host\_ret = (int \*)malloc(1000 \* sizeof(int));

cudaMemcpy(host\_ret, ret, 1000 \* sizeof(int), cudaMemcpyDefault);

for(int i=0; i<1000; i++)

printf("%d: A+B = %d\n", i, host\_ret[i]);

free(host\_ret);

cudaFree(ret);

return 0;

}

This first example combines two numbers together on the GPU with a per-thread ID and returns the values in an array. Without managed memory, both host- and device-side storage for the return values is required (host\_ret and ret in the example), as is an explicit copy between the two using cudaMemcpy().

Compare this with the Unified Memory version of the program, which allows direct access of GPU data from the host. Notice the new cudaMallocManaged() routine, which returns a pointer valid from both host and device code. This allows ret to be used without a separate host\_ret copy, greatly simplifying and reducing the size of the program.

\_\_global\_\_ void AplusB(int \*ret, int a, int b) {

ret[threadIdx.x] = a + b + threadIdx.x;

}

int main() {

int \*ret;

cudaMallocManaged(&ret, 1000 \* sizeof(int));

AplusB<<< 1, 1000 >>>(ret, 10, 100);

cudaDeviceSynchronize();

for(int i=0; i<1000; i++)

printf("%d: A+B = %d\n", i, ret[i]);

cudaFree(ret);

return 0;

}

Finally, language integration allows direct reference of a GPU-declared \_\_managed\_\_ variable and simplifies a program further when global variables are used.

\_\_device\_\_ \_\_managed\_\_ int ret[1000];

\_\_global\_\_ void AplusB(int a, int b) {

ret[threadIdx.x] = a + b + threadIdx.x;

}

int main() {

AplusB<<< 1, 1000 >>>(10, 100);

cudaDeviceSynchronize();

for(int i=0; i<1000; i++)

printf("%d: A+B = %d\n", i, ret[i]);

return 0;

}

Note the absence of explicit cudaMemcpy() commands and the fact that the return array ret is visible on both CPU and GPU.

It is worth a comment on the synchronization between host and device. Notice how in the non-managed example, the synchronous cudaMemcpy() routine is used both to synchronize the kernel (that is, to wait for it to finish running), and to transfer the data to the host. The Unified Memory examples do not call cudaMemcpy() and so require an explicit cudaDeviceSynchronize() before the host program can safely use the output from the GPU.

Note: An alternative here would be to set the environment variable CUDA\_LAUNCH\_BLOCKING=1, ensuring that all kernel launches complete synchronously. This simplifies the code by eliminating all explicit synchronization, but obviously has broader impact on execution behavior as a whole.

### [J.1.2. Data Migration and Coherency](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "um-data-migration)

Unified Memory attempts to optimize memory performance by migrating data towards the device where it is being accessed (that is, moving data to host memory if the CPU is accessing it and to device memory if the GPU will access it). Data migration is fundamental to Unified Memory, but is transparent to a program. The system will try to place data in the location where it can most efficiently be accessed without violating coherency.

The physical location of data is invisible to a program and may be changed at any time, but accesses to the data’s virtual address will remain valid and coherent from any processor regardless of locality. Note that maintaining coherence is the primary requirement, ahead of performance; within the constraints of the host operating system, the system is permitted to either fail accesses or move data in order to maintain global coherence between processors.

### [J.1.3. Multi-GPU Support](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "um-multi-gpu)

Multi-GPU systems are able to use managed memory, but data does not migrate between GPUs. Managed memory allocation behaves identically to unmanaged memory allocated using cudaMalloc(): the current active device is the home for the physical allocation, and all other GPUs receive peer mappings to the memory. This means that other GPUs in the system will access the memory at reduced bandwidth over the PCIe bus.

If peer mappings are not supported between the GPUs in the system, then the managed memory pages are placed in CPU system memory (“zero-copy” memory), and all GPUs will experience PCIe bandwidth restrictions. See [Managed Memory with Multi-GPU Programs](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#um-managed-memory) for details.

### [J.1.4. System Requirements](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "um-requirements)

Unified Memory has three basic requirements:

* a GPU with SM architecture 3.0 or higher (Kepler class or newer)
* a 64-bit host application and operating system, except on Android
* Linux or Windows

### [J.2. Programming Model](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "um-programming-model-hd)

### [J.2.1. Managed Memory Opt In](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "um-opt-in)

CUDA requires a program to opt in to automatic data management by either annotating a \_\_device\_\_ variable with the new \_\_managed\_\_ keyword (see the [Language Integration](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#um-language-integration) section) or by using a new cudaMallocManaged() call to allocate data.

Managed memory must always be allocated on the heap, either with an allocator or by declaring global storage. It is not possible either to associate previously allocated memory with Unified Memory, or to have the Unified Memory system manage a CPU or a GPU stack pointer.

### [J.2.1.1. Explicit Allocation Using cudaMallocManaged()](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "um-explicit-allocation)

Unified memory is most commonly created using an allocation function that is semantically and syntactically similar to the standard CUDA allocator, cudaMalloc(). The function description is as follows:

cudaError\_t cudaMallocManaged(void \*\*devPtr,

size\_t size,

unsigned int flags=0);

The cudaMallocManaged() function allocates size bytes of managed memory on the GPU and returns a pointer in devPtr. The pointer is valid on all GPUs and the CPU in the system, although program accesses to this pointer must obey the concurrency rules of the Unified Memory programming model (see [Coherency and Concurrency](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#um-coherency-hd)). Below is a simple example, showing the use of cudaMallocManaged():

\_\_global\_\_ void printme(char \*str) {

printf(str);

}

int main() {

// Allocate 100 bytes of memory, accessible to both Host and Device code

char \*s;

cudaMallocManaged(&s, 100);

// Note direct Host-code use of "s"

strncpy(s, "Hello Unified Memory\n", 99);

// Here we pass "s" to a kernel without explicitly copying

printme<<< 1, 1 >>>(s);

cudaDeviceSynchronize();

// Free as for normal CUDA allocations

cudaFree(s);

return 0;

}

A program’s behavior is functionally unchanged when cudaMalloc() is replaced with cudaMallocManaged(); however, the program should go on to eliminate explicit memory copies and take advantage of automatic migration. Additionally, dual pointers (one to host and one to device memory) can be eliminated.

In CUDA 6.0, device code is not able to call cudaMallocManaged(). All managed memory must be allocated from the host or at global scope (see the next section). Allocations on the device heap using malloc() in a kernel will not be created in the managed memory space, and so will not be accessible to CPU code.

### [J.2.1.2. Global-Scope Managed Variables Using \_\_managed\_\_](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "um-global-scope)

File-scope and global-scope CUDA \_\_device\_\_ variables may also opt-in to Unified Memory management by adding a new \_\_managed\_\_ annotation to the declaration. These may then be referenced directly from either host or device code, as follows:

\_\_device\_\_ \_\_managed\_\_ int x[2];

\_\_device\_\_ \_\_managed\_\_ int y;

\_\_global\_\_ void kernel() {

x[1] = x[0] + y;

}

int main() {

x[0] = 3;

y = 5;

kernel<<< 1, 1 >>>();

cudaDeviceSynchronize();

printf("result = %d\n", x[1]);

return 0;

}

All semantics of the original \_\_device\_\_ memory space, along with some additional unified-memory-specific constraints, are inherited by the managed variable. See [Compilation with NVCC](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#compilation-with-nvcc)) in the CUDA C Programming Guide for details.

Note that variables marked \_\_constant\_\_ may not also be marked as \_\_managed\_\_; this annotation is reserved for \_\_device\_\_ variables only. Constant memory must be set either statically at compile time or by using cudaMemcpyToSymbol() as usual in CUDA.

### [J.2.2. Coherency and Concurrency](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "um-coherency-hd)

### [J.2.2.1. GPU Exclusive Access To Managed Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "um-gpu-exclusive)

To ensure coherency, the Unified Memory programming model puts constraints on data accesses while both the CPU and GPU are executing concurrently. In effect, the GPU has exclusive access to all managed data while any kernel operation is executing, regardless of whether the specific kernel is actively using the data. When managed data is used with cudaMemcpy\*() or cudaMemset\*(), the system may choose to access the source or destination from the host or the device, which will put constraints on concurrent CPU access to that data while the cudaMemcpy\*() or cudaMemset\*() is executing. See [Memcpy()/Memset() Behavior With Managed Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#um-memcpy-memset) for further details.

In general, it is not permitted for the CPU to access any managed allocations or variables while the GPU is active. Concurrent CPU/GPU accesses, even to different managed memory allocations, will cause a segmentation fault because the page is considered inaccessible to the CPU.

\_\_device\_\_ \_\_managed\_\_ int x, y=2;

\_\_global\_\_ void kernel() {

x = 10;

}

int main() {

kernel<<< 1, 1 >>>();

y = 20; // ERROR: CPU access concurrent with GPU

cudaDeviceSynchronize();

return 0;

}

In example above, the GPU program kernel is still active when the CPU touches y. (Note how it occurs before cudaDeviceSynchronize().) This access is invalid even though the CPU is accessing different data than the GPU. The program must explicitly synchronize with the GPU before accessing y:

\_\_device\_\_ \_\_managed\_\_ int x, y=2;

\_\_global\_\_ void kernel() {

x = 10;

}

int main() {

kernel<<< 1, 1 >>>();

cudaDeviceSynchronize();

y = 20; // Success – GPU is idle so access is OK

return 0;

}

As this example shows, a CPU thread may not access any managed data in between performing a kernel launch and a subsequent synchronization call, regardless of whether the GPU kernel actually touches that same data (or any managed data at all). The mere potential for concurrent CPU and GPU access is sufficient for a process-level exception to be raised.

Note that if memory is dynamically allocated with cudaMallocManaged() or cuMemAllocManaged() while the GPU is active, the behavior of the memory is unspecified until additional work is launched or the GPU is synchronized. Attempting to access the memory on the CPU during this time may or may not cause a segmentation fault. This does not apply to memory allocated using the flag cudaMemAttachHost or CU\_MEM\_ATTACH\_HOST.

### [J.2.2.2. Explicit Synchronization and Logical GPU Activity](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "um-explicit-synchronization)

Note that explicit synchronization is required even if kernel runs quickly and finishes before the CPU touches y in the above example. Unified Memory uses logical activity to determine whether the GPU is idle. This aligns with the CUDA programming model, which specifies that a kernel can run at any time following a launch and is not guaranteed to have finished until the host issues a synchronization call.

Any function call that logically guarantees the GPU completes its work is valid. This includes cudaDeviceSynchronize(); cudaStreamSynchronize() and cudaStreamQuery() (provided it returns cudaSuccess and not cudaErrorNotReady) where the specified stream is the only stream still executing on the GPU; cudaEventSynchronize() and cudaEventQuery() in cases where the specified event is not followed by any device work; as well as uses of cudaMemcpy() and cudaMemset() that are documented as being fully synchronous with respect to the host.

Dependencies created between streams will be followed to infer completion of other streams by synchronizing on a stream or event. Dependencies can be created via cudaStreamWaitEvent() or implicitly when using the default (NULL) stream.

It is legal for the CPU to access managed data from within a stream callback, provided no other stream that could potentially be accessing managed data is active on the GPU. In addition, a callback that is not followed by any device work can be used for synchronization: for example, by signaling a condition variable from inside the callback; otherwise, CPU access is valid only for the duration of the callback(s).

There are several important points of note:

* It is always permitted for the CPU to access non-managed zero-copy data while the GPU is active.
* The GPU is considered active when it is running any kernel, even if that kernel does not make use of managed data. If a kernel might use data, then access is forbidden.
* There are no constraints on concurrent inter-GPU access of managed memory, other than those that apply to multi-GPU access of non-managed memory.
* There are no constraints on concurrent GPU kernels accessing managed data.

Note how the last point allows for races between GPU kernels, as is currently the case for non-managed GPU memory. As mentioned previously, managed memory functions identically to non-managed memory from the perspective of the GPU. The following code example illustrates these points:

int main() {

cudaStream\_t stream1, stream2;

cudaStreamCreate(&stream1);

cudaStreamCreate(&stream2);

int \*non\_managed, \*managed, \*also\_managed;

cudaMallocHost(&non\_managed, 4); // Non-managed, CPU-accessible memory

cudaMallocManaged(&managed, 4);

cudaMallocManaged(&also\_managed, 4);

// Point 1: CPU can access non-managed data.

kernel<<< 1, 1, 0, stream1 >>>(managed);

\*non\_managed = 1;

// Point 2: CPU cannot access any managed data while GPU is busy.

// Note we have not yet synchronized, so "kernel" is still active.

\*also\_managed = 2; // Will issue segmentation fault

// Point 3: Concurrent GPU kernels can access the same data.

kernel<<< 1, 1, 0, stream2 >>>(managed);

// Point 4: Multi-GPU concurrent access is also permitted.

cudaSetDevice(1);

kernel<<< 1, 1 >>>(managed);

return 0;

}

### [J.2.2.3. Managing Data Visibility and Concurrent CPU + GPU Access](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "um-managing-data)

Until now it was assumed that any active kernel may use any managed memory and that it was invalid to use managed memory from the CPU while a kernel is active. Here we present a system for finer-grained control of managed memory.

The CUDA programming model provides streams as a mechanism for programs to indicate dependence and independence among kernel launches. Kernels launched into the same stream are guaranteed to execute consecutively, while kernels launched into different streams are permitted to execute concurrently. Streams describe independence between work items and hence allow potentially greater efficiency through concurrency.

Unified Memory builds upon the stream-independence model by allowing a CUDA program to explicitly associate managed allocations with a CUDA stream. In this way, the programmer indicates the use of data by kernels based on whether they are launched into a specified stream or not. This enables opportunities for concurrency based on program-specific data access patterns. A new function exists to control this:

cudaError\_t cudaStreamAttachMemAsync(cudaStream\_t stream,

void \*ptr,

size\_t length=0,

unsigned int flags=0);

The cudaStreamAttachMemAsync() function associates length bytes of memory starting from ptr with the specified stream. (Currently, length must always be 0 to indicate that the entire region should be attached.) Because of this association, the Unified Memory system allows CPU access to this memory region so long as all operations in stream have completed, regardless of whether other streams are active. In effect, this constrains exclusive ownership of the managed memory region by an active GPU to per-stream activity instead of whole-GPU activity.

Most importantly, if an allocation is not associated with a specific stream, it is visible to all running kernels regardless of their stream. This is the default visibility for a cudaMallocManaged() allocation or a \_\_managed\_\_ variable; hence, the simple-case rule that the CPU may not touch the data while any kernel is running.

By associating an allocation with a specific stream, the program makes a guarantee that only kernels launched into that stream will touch that data. No error checking is performed by the Unified Memory system: it is the programmer’s responsibility to ensure that guarantee is honored.

In addition to allowing greater concurrency, the use of cudaStreamAttachMemAsync() can (and typically does) enable data transfer optimizations within the Unified Memory system that may affect latencies and other overhead.

### [J.2.2.4. Stream Association Examples](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "um-stream-association)

Associating data with a stream allows fine-grained control over CPU + GPU concurrency, but what data is visible to which streams must be kept in mind. Looking at the earlier synchronization example:

\_\_device\_\_ \_\_managed\_\_ int x, y=2;

\_\_global\_\_ void kernel() {

x = 10;

}

int main() {

cudaStream\_t stream1;

cudaStreamCreate(&stream1);

cudaStreamAttachMemAsync(stream1, &y, 0, cudaMemAttachHost);

cudaDeviceSynchronize(); // Wait for Host attachment to occur.

kernel<<< 1, 1, 0, stream1 >>>(); // Note: Launches into stream1.

y = 20; // Success – a kernel is running but “y”

// has been associated with no stream.

return 0;

}

Here we explicitly associate y with host accessibility, thus enabling access at all times from the CPU. (As before, note the absence of cudaDeviceSynchronize() before the access.) Accesses to y by the GPU running kernel will now produce undefined results.

Now, here's an example of where things can go wrong. This may seem like it should be okay, but it’s not:

\_\_device\_\_ \_\_managed\_\_ int x, y=2;

\_\_global\_\_ void kernel() {

x = 10;

}

int main() {

cudaStream\_t stream1;

cudaStreamCreate(&stream1);

cudaStreamAttachMemAsync(stream1, &x);// Associate “x” with stream1.

cudaDeviceSynchronize(); // Wait for “x” attachment to occur.

kernel<<< 1, 1, 0, stream1 >>>(); // Note: Launches into stream1.

y = 20; // ERROR: “y” is still associated globally

// with all streams by default

return 0;

}

Note how the access to y will cause an error because, even though x has been associated with a stream, we have told the system nothing about who can see y. The system therefore conservatively assumes that kernel might access it and prevents the CPU from doing so.

### [J.2.2.5. Stream Attach With Multithreaded Host Programs](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "um-stream-attach)

The primary use for cudaStreamAttachMemAsync() is to enable independent task parallelism using CPU threads. Typically in such a program, a CPU thread creates its own stream for all work that it generates because using CUDA’s NULL stream would cause dependencies between threads.

The default global visibility of managed data to any GPU stream can make it difficult to avoid interactions between CPU threads in a multi-threaded program. Function cudaStreamAttachMemAsync() is therefore used to associate a thread’s managed allocations with that thread’s own stream, and the association is typically not changed for the life of the thread.

Such a program would simply add a single call to cudaStreamAttachMemAsync() to use unified memory for its data accesses:

// This function performs some task, in its own private stream.

void run\_task(int \*in, int \*out, int length) {

// Create a stream for us to use.

cudaStream\_t stream;

cudaStreamCreate(&amp;stream);

// Allocate some managed data and associate with our stream.

// Note the use of the host-attach flag to cudaMallocManaged();

// we then associate the allocation with our stream so that

// our GPU kernel launches can access it.

int \*data;

cudaMallocManaged((void \*\*)&data, length, cudaMemAttachHost);

cudaStreamAttachMemAsync(stream, data);

cudaStreamSynchronize(stream);

// Iterate on the data in some way, using both Host & Device.

for(int i=0; i<N; i++) {

transform<<< 100, 256, 0, stream >>>(in, data, length);

cudaStreamSynchronize(stream);

host\_process(data, length); // CPU uses managed data.

convert<<< 100, 256, 0, stream >>>(out, data, length);

}

cudaStreamSynchronize(stream);

cudaStreamDestroy(stream);

cudaFree(data);

}

In this example, the allocation-stream association is established just once, and then data is used repeatedly by both the host and device. The result is much simpler code than occurs with explicitly copying data between host and device, although the result is the same.

### [J.2.2.6. Advanced Topic: Modular Programs and Data Access Constraints](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "um-advanced-modular)

In the previous example cudaMallocManaged() specifies the cudaMemAttachHost flag, which creates an allocation that is initially invisible to device-side execution. (The default allocation would be visible to all GPU kernels on all streams.) This ensures that there is no accidental interaction with another thread’s execution in the interval between the data allocation and when the data is acquired for a specific stream.

Without this flag, a new allocation would be considered in-use on the GPU if a kernel launched by another thread happens to be running. This might impact the thread’s ability to access the newly allocated data from the CPU (for example, within a base-class constructor) before it is able to explicitly attach it to a private stream. To enable safe independence between threads, therefore, allocations should be made specifying this flag.

Note: An alternative would be to place a process-wide barrier across all threads after the allocation has been attached to the stream. This would ensure that all threads complete their data/stream associations before any kernels are launched, avoiding the hazard. A second barrier would be needed before the stream is destroyed because stream destruction causes allocations to revert to their default visibility. The cudaMemAttachHost flag exists both to simplify this process, and because it is not always possible to insert global barriers where required.

### [J.2.2.7. Memcpy()/Memset() Behavior With Managed Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "um-memcpy-memset)

Since managed memory can be accessed from either the host or the device, cudaMemcpy\*() relies on the type of transfer, specified using cudaMemcpyKind, to determine whether the data should be accessed as a host pointer or a device pointer.

If cudaMemcpyHostTo\* is specified and the source data is managed, then it will be accessed from the device if it has global visibility or if it’s associated with the stream being used for the copy operation; otherwise, it will be accessed from the host. Similar rules apply to the destination when cudaMemcpy\*ToHost is specified and the destination is managed memory. Note that a segmentation fault can occur during the copy operation if data is being accessed from the host and its associated stream is active on the GPU.

If cudaMemcpyDeviceTo\* is specified and the source data is managed, then it will be accessed from the device. The source must either have global visibility or it must be associated with the copy stream; otherwise, an error is returned. Similar rules apply to the destination when cudaMemcpy\*ToDevice is specified and the destination is managed memory.

If cudaMemcpyDefault is specified, then managed data will be accessed from the device if it has global visibility or if it’s associated with the copy stream; otherwise, it will be accessed from the host.

When using cudaMemset\*() with managed memory, the data is always accessed from the device. The data must either have global visibility, or it must be associated with the stream being used for the cudaMemset() operation; otherwise, an error is returned.

When data is accessed from the device either by cudaMemcpy\*() or cudaMemset\*(), the stream of operation is considered to be active on the GPU. During this time, any CPU access of data that is associated with that stream or data that has global visibility, will result in a segmentation fault. The program must synchronize appropriately to ensure the operation has completed before accessing any associated data from the CPU.

### [J.2.3. Language Integration](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "um-language-integration)

Users of the CUDA Runtime API who compile their host code using nvcc have access to additional language integration features, such as shared symbol names and inline kernel launch via the <<<...>>> operator. Unified Memory adds one additional element to CUDA’s language integration: variables annotated with the \_\_managed\_\_ keyword can be referenced directly from both host and device code.

The following example, seen earlier in [Simplifying GPU Programming](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#um-simplifying), illustrates a simple use of \_\_managed\_\_ global declarations:

// Managed variable declaration is an extra annotation with \_\_device\_\_

\_\_device\_\_ \_\_managed\_\_ int x;

\_\_global\_\_ void kernel() {

// Reference "x" directly - it's a normal variable on the GPU.

printf( "GPU sees: x = %d\n" , x);

}

int main() {

// Set "x" from Host code. Note it's just a normal variable on the CPU.

x = 1234;

// Launch a kernel which uses "x" from the GPU.

kernel<<< 1, 1 >>>();

cudaDeviceSynchronize();

return 0;

}

The new capability introduced with \_\_managed\_\_ variables is that the symbol is available in both device code and in host code without the need to dereference a pointer, and the data is shared by all. This makes it particularly easy to exchange data between host and device programs without the need for explicit allocations or copying.

Semantically, the behavior of \_\_managed\_\_ variables is identical to that of storage allocated via cudaMallocManaged(). Data is hosted in physical GPU storage and is visible to all GPUs in the system as well as the CPU. Stream visibility defaults to cudaMemAttachGlobal, but may be constrained using cudaStreamAttachMemAsync().

A valid CUDA context is necessary for the correct operation of \_\_managed\_\_ variables. Accessing \_\_managed\_\_ variables can trigger CUDA context creation if a context for the current device hasn’t already been created. In the example above, accessing x before the kernel launch triggers context creation on device 0. In the absence of that access, the kernel launch would have triggered context creation.

C++ objects declared as \_\_managed\_\_ are subject to certain specific constraints, particularly where static initializers are concerned. Please refer to [C/C++ Language Support](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#c-cplusplus-language-support) in the CUDA C Programming Guide for a list of these constraints.

### [J.2.3.1. Host Program Errors with \_\_managed\_\_ Variables](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "um-host-program-errors)

The use of \_\_managed\_\_ variables depends upon the underlying Unified Memory system functioning correctly. Incorrect functioning can occur if, for example, the CUDA installation failed or if the CUDA context creation was unsuccessful.

When CUDA-specific operations fail, typically an error is returned that indicates the source of the failure. Using \_\_managed\_\_ variables introduces a new failure mode whereby a non-CUDA operation (for example, CPU access to what should be a valid host memory address) can fail if the Unified Memory system is not operating correctly. Such invalid memory accesses cannot easily be attributed to the underlying CUDA subsystem, although a debugger such as cuda-gdb will indicate that a managed memory address is the source of the failure.

### [J.2.4. Querying Unified Memory Support](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "um-querying-um-hd)

### [J.2.4.1. Device Properties](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "um-device-properties)

Unified Memory is supported only on devices with compute capability 3.0 or higher. A program may query whether a GPU device supports managed memory by using cudaGetDeviceProperties() and checking the new managedMemSupported property. The capability can also be determined using the individual attribute query function cudaDeviceGetAttribute() with the attribute cudaDevAttrManagedMemSupported.

Either property will be set to 1 if managed memory allocations are permitted on the GPU and under the current operating system. Note that Unified Memory is not supported for 32-bit applications (unless on Android), even if a GPU is of sufficient capability.

### [J.2.4.2. Pointer Attributes](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "um-pointer-attributes)

To determine if a given pointer refers to managed memory, a program can call cudaPointerGetAttributes() and check the value of the isManaged attribute. This attribute is set to 1 if the pointer refers to managed memory and to 0 if not.

### [J.2.5. Advanced Topics](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "um-advanced-topics-hd)

### [J.2.5.1. Managed Memory with Multi-GPU Programs](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "um-managed-memory)

Managed allocations are automatically visible to all GPUs in a system via the peer-to-peer capabilities of the GPUs. If peer mappings are not available (for example, between GPUs of different architectures), then the system will fall back to using zero-copy memory in order to guarantee data visibility. This fallback happens automatically, regardless of whether both GPUs are actually used by a program.

If only one GPU is actually going to be used, it is necessary to set the CUDA\_VISIBLE\_DEVICES environment variable before launching the program. This constrains which GPUs are visible and allows managed memory to be allocated in GPU memory. On a system with more than two GPUs, so long as peer mapping is supported between all visible GPUs, managed allocations will not fall back to zero-copy memory.

Alternatively, users can also set CUDA\_MANAGED\_FORCE\_DEVICE\_ALLOC to a non-zero value to force the driver to always use device memory for physical storage. When this environment variable is set to a non-zero value, all devices used in that process that support managed memory have to be peer-to-peer compatible with each other. The error ::cudaErrorInvalidDevice will be returned if a device that supports managed memory is used and it is not peer-to-peer compatible with any of the other managed memory supporting devices that were previously used in that process, even if ::cudaDeviceReset has been called on those devices. These environment variables are described in Appendix [CUDA Environment Variables](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#env-vars).

### [J.2.5.2. Using fork() with Managed Memory](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "um-fork-managed-memory)

The Unified Memory system does not allow sharing of managed memory pointers between processes. It will not correctly manage memory handles that have been duplicated via a fork() operation. Results will be undefined if either the child or parent accesses managed data following a fork().

It is safe, however, to fork() a child process that then immediately exits via an exec() call, because the child drops the memory handles and the parent becomes the sole owner once again. It is not safe for the parent to exit and leave the child to access the handles.

## [Notices](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "notices-header)

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[1](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "fnsrc_1) 4 for GeForce GPUs

[2](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "fnsrc_2) 8 for GeForce GPUs

[3](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "fnsrc_3) 32 for GeForce GPUs

[4](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "fnsrc_4) 4 for GeForce GPUs

[5](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "fnsrc_5) 8 for GeForce GPUs

[1](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "fnsrc_6) Dynamically created texture and surface objects are an addition to the CUDA memory model introduced with CUDA 5.0. Please see the CUDA Programming Guide for details.

[7](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "fnsrc_7) This does not apply to entities that may be defined in more than one translation unit, such as compiler generated template instantiations.

[8](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "fnsrc_8) supported with architectures >= sm\_35

[9](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "fnsrc_9) At present, the -std=c++11 flag is supported only for the following host compilers : gcc version >= 4.7, clang

[10](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "fnsrc_10) including operator()

[11](http://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html" \l "fnsrc_11) The restrictions are the same as with a non-constexpr callee function.

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